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RELIABILITY OF LINEAR INTEGRATED CIRCUITS IN CERAMIC AND PLASTIC PACKAGES

General Electric Company

Rome Air Development Center
Air Force Systems Command
Griffiss Air Force Base, New York

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FOREWORD

The information presented in this report resulted from work performed under contract F30602-71-C-0223, Job Order Number 55190622, for Rome Air Development Center, Griffiss Air Force Base, New York, by General Electric Company, Semiconductor Products Department, Syracuse, New York. Mr. Vincent C. Kapfer (RBRP) was the RADC Project Engineer.

The program was under the overall direction of Program Manager E.A. Herr, Manager of Reliability Engineering, Semiconductor Products Department. This final report was prepared by B.L. Bair, A. Fox, A. Poe, and W. Brouilette. Others who contributed to the work effort of the program included S.S. Barnhart, J.P. Davies, G. Kamerson, R.R. Langendorfer, J. McDonald, T. Kupinski, G. Vrooman, and R. Warr. The program was performed between 17 March 1971 and 29 August 1972.

This technical report has been reviewed and is approved.

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ABSTRACT

This final report describes the results obtained from a contract on a study of the reliability of linear integrated circuits. The objective of the contract was to investigate and determine the basic failure mechanisms associated with linear microcircuits fabricated in ceramic and plastic packages.

The type of test vehicle chosen for this program was the 741 operational amplifier. Two of the five vehicles chosen for the program were manufactured by one supplier with half of the devices encapsulated in ceramic packages and the other half encapsulated in silicone plastic. The devices fabricated by the other supplier included three packaging variations; the first was a ceramic package with conventional metalization and wire bonding, the second was a plastic encapsulated package with conventional metalization and wire bonding, and the third was a plastic encapsulated package utilizing a gang bonding technique. In addition, Test Element Groups (TEGs) were fabricated using the last three packaging techniques. These were selectively stressed to provide a measure of the sensitivity of TEG parameters to the selected stresses.

The test plan for these devices was designed to include both step-stress and long term stress-in-time tests. The stresses were chosen to identify any failure mechanisms that could be activated by high temperatures, temperature cycling, salt atmosphere, steam pressure and high humidity environments. Over 1000 microcircuits and about 285 TEGs were measured for electrical parameters

and then were stressed on this program. The device responses were analyzed during and after the stress program and representative candidates were then chosen for detailed failure analyses. Summaries of the results of the stress tests and failure analyses along with the conclusions from these results are included in this report.

Technical Evaluation

The objective of this study was to investigate and determine the basic failure mechanisms associated with state-of-the-art production linear microcircuits fabricated in ceramic and plastic packages. There were five package variations of the 741 operational amplifier obtained from two vendors. These packages were representative of major manufacturers' products.

The increased usage of linear integrated circuits to perform a variety of functions in military equipments, prompted this effort. In order to assess the reliability of these devices, Class C screens as per MIL-STD-883 were initially performed on the circuits prior to stressing. The devices were then subjected to a series of stress tests which were designed to compare the reliability performance of the linear amplifier in the various package configurations.

A significant finding of this effort was the selection of the electrical parameters which were utilized during the stress program. Two of these parameters, i.e., input offset voltage [V_{IO}] and power supply current drain [I_{PS}] were most sensitive to the effects of moisture, surface contamination, and resistance change in the lead bond metallization system.

These parameters are being used in MIL-M-38510/101B slash sheet. The results of this effort show that of the parameters listed in the detailed parameter specifications for linear microcircuits, V_{IO}-input offset voltage and I_{PS}-power supply drain current are the most sensitive indicators of degradation.

Results of this study indicate that the response of the circuit to the severity of the specific stresses reacted differently depending upon the package type. For the most severe stress, Cell 1 "Temperature With Bias," all device types were responsive to this stress. All devices subjected to Cell 6 "Temperature Cycling" (air-to-air), were failure free. However, after being subjected to 50 cycles of thermal shock (liquid-to-liquid), all of these devices, with the exception of Type D devices encapsulated in silicone plastic, showed some degradation. For all of the above types of devices, temperature cycling without bias is an ineffective stress test.

Results of the special cool-down and electrical measurement procedures, suggested by RADC for devices in stress Cell 1 "Temperature Step Stress With Bias," did not show any surface inversion problems in the 741 operational amplifiers. This surface inversion problem was detected earlier at RADC on some 709 operational amplifiers at elevated temperatures with bias.

Hot ethylene glycol, which was used in the thermal shock tests, attacked the ceramic package glass frit seal used in the Type B devices. These devices were degraded by a residue build-up of the glass constituents which were deposited on the device chip causing excessive leakage. This finding indicates that a proper liquid should be chosen for the thermal shock tests to prevent the attack of the structural materials of the package.

No additional contractual efforts will be initiated in the linear amplifier area at present. However, an in-house program to extend the work done under this contract will include several additional vendors' devices as well as devices obtained from this effort.

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SECTION I

INTRODUCTION

A. BACKGROUND INFORMATION

The objective of this program was to investigate and determine the basic failure mechanisms associated with linear microcircuits fabricated in ceramic and plastic packages. A series of stress tests were performed followed by comprehensive failure analyses on selected devices. This objective was met.

One area that has been of great concern has been the potential degradation of any device when it is subjected to humidity. The mechanisms that could be observed involve the penetration of water vapor through the package or along the device leads. If this occurs, it would be possible to observe ionic conduction external to the pellet surface or on the pellet surface, and surface inversion or channeling. The indicators of this type of change include increases in the collector to base leakage current, shift in the small signal current gain and shifts in the collector to base breakdown voltage. The presence of humidity could also result in corrosion, as evidenced by a chemical attack of the internal leads, the metalization, the bonds (intermetallics), the external leads and the silicon pellet. Any attack of the chip would usually be due to the presence of residual salts, and/or ammonia ions or anhydrides in the case of plastic encapsulations. These latter impurities can be prevented by a combination of material selection and good in process control. Several of these failure mechanisms are also found in ceramic packaged devices.

It is also necessary to make certain of the uniformity, purity, chemical composition and stability, and the physical properties of the encapsulating material. If these areas are not adequately controlled, it would be possible to observe problems with the interactions of the chip surface and the encapsulant (leading to channeling), an increased sensitivity to humidity and changes in the thermal impedance. Additional problem areas for plastic encapsulations could include the thermal coefficient of expansion of the several materials and changes in the mechanical strength of the encapsulating material. Some of the plastics which have been suggested for use as encapsulants have been limited to operation or storage at temperatures below 150°C. This has been a limitation for the usual military specification, but several epoxies and silicones have been tested and are presently being evaluated at temperatures in excess of 150°C.

However, the solid plastic encapsulation provides a much greater ability for the completed device to withstand mechanical stresses. The solid encapsulant provides good thermal transfer, since there is contact to the entire surface of the pellet and the internal leads. Such complete contact increases the current handling capability of the pellet because of the improved thermal conductivity of the solid encapsulant over that of the internal gas environment which is standard in metal can transistors. The solid encapsulation also provides complete mechanical support of the internal components and eliminates any possible problems with loose particles.

B. BASIC PROGRAM TEST VEHICLES

The test vehicles used on this program were all versions of the 741 Operational Amplifier, which is a monolithic, high performance

operational amplifier with high impedance differential inputs and a low impedance output. Five versions of this device were used of which three were fabricated by one vendor and two were fabricated by a second vendor.

The two types of devices supplied by the second vendor included one version in a ceramic package and one version in a silicone plastic encapsulation. The three versions fabricated by the first supplier included a standard chip mounted in a ceramic package, a standard chip in an epoxy plastic package and one using a glassivated gang bonded chip in an epoxy plastic encapsulation. Four of the package types were 14 lead, dual-in-line packages and the silicone plastic device was in an 8 lead dual-in-line package. The devices are described in greater detail in the next section of this report.

SECTION II

DEVICE DESCRIPTION

A. GENERAL

The 741 operational amplifier is a high performance amplifier with internal compensation consisting of a 30 pF capacitor. An equivalent schematic diagram is shown in Figure 1. The 741 is essentially a three stage amplifier with a high gain input stage, a high gain driver stage and a Class AB output stage. To achieve low input bias currents, a combination of high beta NPN and a low beta PNP transistors is used in the input circuit. Because the emitter-base breakdown voltages of the lateral PNP transistors (Q3 and Q4) are large, an additional advantage is gained in that the input can withstand $\pm$ 30 volt differential input voltages without breaking down the base-emitter junctions of Q1 and/or Q2. Transistors Q5 and Q6 are used as active loads giving values of about 2 megohms. The operating collector current of the input stage is determined by Q8, Q9 and Q10.

A Darlington driver, consisting of Q16 and Q17, is used to prevent loading of the first stage. The driving stage (Q13 and Q17) provides the proper signals to the output, which is a conventional complementary symmetry circuit consisting of Q14 and Q20.

There is built in short circuit protection which limits the output current to approximately 25 milliamperes at room temperature. No damage will occur to the 741 if the output is shorted either to

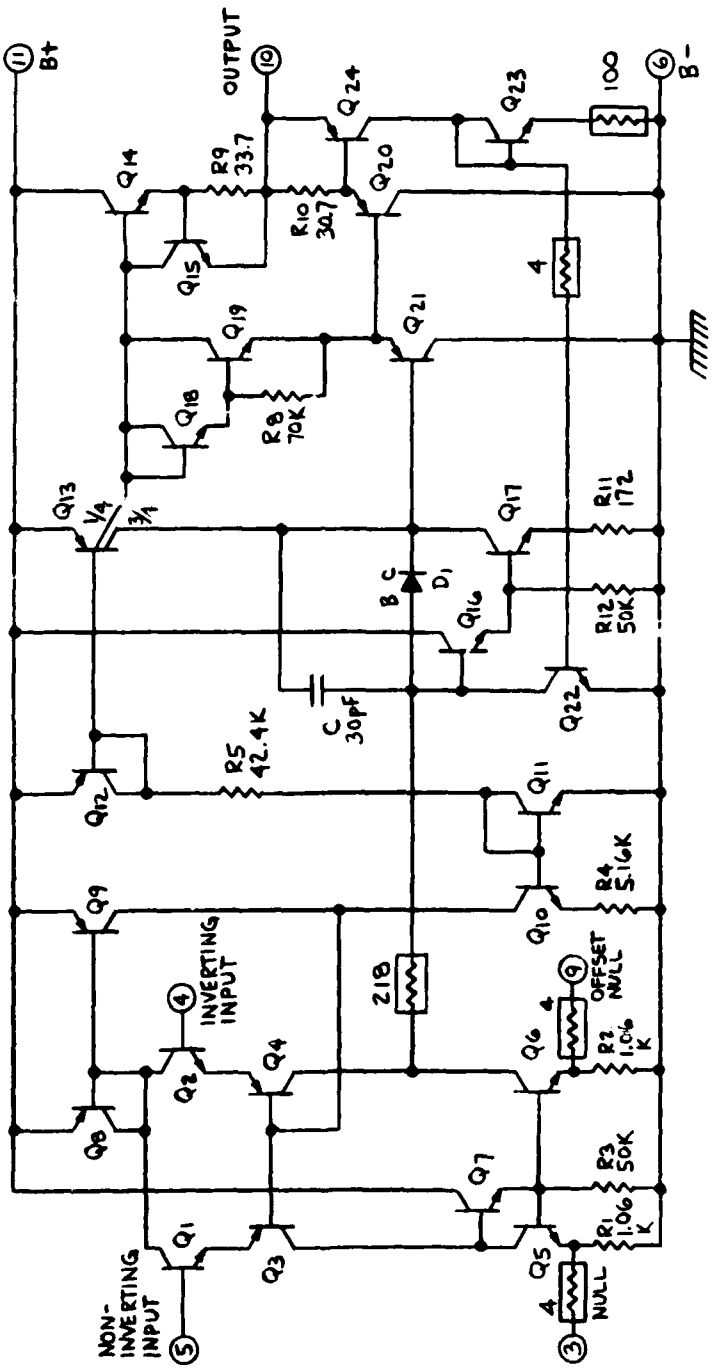


Figure 1 741 Operational Amplifier Equivalent Schematic

ground or to the positive or negative supply. The input will not be damaged even if it is shorted to plus or minus 15 volts. No external frequency compensation is required for closed loop operation, but may be added between pins 9 and 10 if a reduced gain bandwidth product is desired.

B. SPECIFICATIONS

The general electrical characteristics of the 741 amplifier are shown in Figure 2. These include static and dynamic characteristics at room temperature and extreme temperatures. The characteristics and planned limits which were used to monitor the device performance during the program are described in the test plan section of this report (Section III).

C. MANUFACTURING VARIATIONS

As mentioned earlier, in the Introduction, there were five packaging variations employed for the 741 operational amplifier and three of these variations were used for the Test Element Group, TEG. To avoid repeated descriptions of these variations, a nomenclature guide was developed which will be used in the balance of this report. The adopted nomenclature is:

- Type A: First manufacturer, 741 Integrated Circuit (IC) in a ceramic package with a metal lid, flying wire bonding,
- Type AT: First manufacturer, TEG in a ceramic package with a metal lid, flying wire bonding,
- Type B: Second manufacturer, 741 Integrated Circuit (IC) in a ceramic package with a ceramic lid, flying wire bonding,
- Type C: First manufacturer, 741 Integrated Circuit (IC) in an epoxy package, flying wire bonding,

ELECTRICAL CHARACTERISTICS

$V_{CC+} = V_{CC-} = 15V$, ($T_A = 25^{\circ}C$ UNLESS OTHERWISE SPECIFIED)

SYMBOL	PARAMETER CONDITIONS	PRODUCTION MIN.	TYP.	MAX.	UNITS
V_{IO}	INPUT OFFSET VOLTAGE $R_S \leq 10K\Omega$		1.0	5.0	mV
I_{IO}	INPUT OFFSET CURRENT		2.0	200	nA
I_{IB}	INPUT BIAS CURRENT		80	500	nA
R_I	INPUT RESISTANCE	0.3	2.0		MΩ
C_I	INPUT CAPACITANCE		1.4		pF
$V_{IO(ADJ)\pm}$	OFFSET VOLTAGE ADJUSTMENT RANGE		±15		mV
$V_{IPP\pm}$	INPUT VOLTAGE RANGE	±12	±13		V
CMRR	COMMON MODE REJECTION RATIO $R_S \leq 10K\Omega$	70	90		dB
PSRR	SUPPLY VOLTAGE REJECTION RATIO $R_S \leq 10K\Omega$		30	150	μV/V
$A_{VS(\pm)}$	LARGE SIGNAL VOLTAGE GAIN $R_L \geq 2K$, $V_{OUT} = \pm 10V$	50K	200K		
$V_{OPP\pm}$	OUTPUT VOLTAGE SWING $R_L \leq 10K\Omega$	±12	±14		V
	$R_L \leq 2K\Omega$	±10	±13		V
R_O	OUTPUT RESISTANCE		75		Ω
I_{OS}	OUTPUT SHORT-CIRCUIT CURRENT		25		mA
P_D	POWER CONSUMPTION		50	85	mW
T_R	TRANSIENT RESPONSE (UNITY GAIN) $V_{IN} = 20$ mV, $R_L = 2K$, $C_L \leq 100$ pF				
	RISETIME		0.3		μS
	OVERSHOOT		5.0		%
SR	SLEW RATE $R_L \geq 2K$, $C_C = 30$ pF		0.5		V/μS
	THE FOLLOWING SPECIFICATIONS APPLY FOR $-55^{\circ}C \leq T \leq +125^{\circ}C$				
V_{IO}	INPUT OFFSET VOLTAGE $R_S \leq 10K\Omega$		1.0	6.0	mV
I_{IO}	INPUT OFFSET CURRENT $T_A = +125^{\circ}C$		7.0	200	nA
	$T_A = -55^{\circ}C$		85	500	
I_{IB}	INPUT BIAS CURRENT $T_A = +125^{\circ}C$		0.03	0.5	μA
	$T_A = -55^{\circ}C$		0.3	1.5	
$A_{VS(\pm)}$	LARGE SIGNAL VOLTAGE GAIN $R_L \geq 2K$, $V_{OUT} = \pm 10V$	25K			
$V_{OPP\pm}$	OUTPUT VOLTAGE SWING $R_L \geq 10K\Omega$	±12	±14		V
$V_{OPP\pm}$	OUTPUT VOLTAGE SWING $R_L \geq 2K\Omega$	±10	±13		V
$V_{IPP\pm}$	INPUT VOLTAGE RANGE	±12	±13		V
CMRR	COMMON MODE REJECTION RATIO $R_S \leq 10K\Omega$	70	90		dB
PSRR	SUPPLY VOLTAGE REJECTION RATIO $R_S \leq 10K\Omega$		30	150	μV/V
P_D	POWER CONSUMPTION $T_A = +125^{\circ}C$		45	75	mW
P_D	POWER CONSUMPTION $T_A = -55^{\circ}C$		60	100	mW

Figure 2 741 Operational Amplifier Specification

- Type CT: First manufacturer, TEG in an epoxy plastic package, flying wire bonding,

- Type D: Second manufacturer, 741 Integrated Circuit (IC) in a silicone plastic package, flying wire bonding,

- Type E: First manufacturer, 741 Integrated Circuit (IC) in an epoxy plastic package, gang bonding,

- Type ET: First manufacturer, TEG in an epoxy plastic package gang bonding.

All of the different types used aluminum metalization on the chip, with the exception of the pad area for the Type E devices - which will be described later in this report. Study of the preceding listing will indicate that Types A, C and E (and the associated TEGs) were supplied by one manufacturer and that Type B and D were supplied by the second manufacturer. The construction features are listed in detail in Table I.

A topological composite of the Types A, C and E 741 Operational Amplifier, with the component elements identified, is shown in Figure 3. The composite was not available for Types B and D 741's, but a photograph of the chip top view is shown in Figure 4. The TEG topological composite is shown in Figure 5 and the TEG schematic, including the external pin connections, is shown in Figure 6. All of the 741s are pin-for-pin interchangeable and comparison of Figures 3 and 4 reveals that there are some minor differences, but the two manufacturers' versions are basically similar in layout. This similarity was of aid in performing the failure analyses following the stress test program. Photographs of the completed devices, x-rays of the interior construction and a drawing of the gang bond assembly are all shown in Figure 11.

TABLE 1 741 MANUFACTURING VARIATIONS

TYPE	A OR AT	B	C OR CT	D	E OR ET
MANUFACTURER	1	2	1	2	1
PACKAGE	Ceramic 14 Lead DIP	Ceramic 14 Lead DIP	Epoxy 14 Lead DIP	Silicone 8 Lead DIP	Epoxy 14 Lead DIP
LID	Metal	Ceramic	-	-	-
LID SEAL	Braze	Glass Frit	-	-	-
CHIP MOUNT	Eutectic No Preform	Eutectic	Eutectic with Preform	Eutectic	Floating
CHIP COATING	None	None	Silicone Rubber	Silicone Rubber	None
GLASSIVATION	None	Silox	None	None	Silox
METALIZATION	Al - 1 mil	Al - 1 mil	Al - 1 mil	Al - 1 mil	Al - 1 mil
LEAD FRAME	Gold Nickel Alloy	Nickel Alloy	Copper, Silver Plated	Nickel Alloy, Tin Dipped, Gold Plated	Copper, Tin Plated
INTERNAL LEADS	1 mil Au Flying Wire	1 mil Al. Flying Wire	1.5 mil Au Flying Wire	1 mil Au Flying Wire	Copper 4 X 1.4 mil
LEAD BONDING	USB Bonds	USB Bonds	TCB Ball Bonds	TCB Ball Bonds	Gold-Tin Impulse Soldered
BONDING PAD	Aluminum	Aluminum	Aluminum	Aluminum	Aluminum, Buffer Metal, Gold

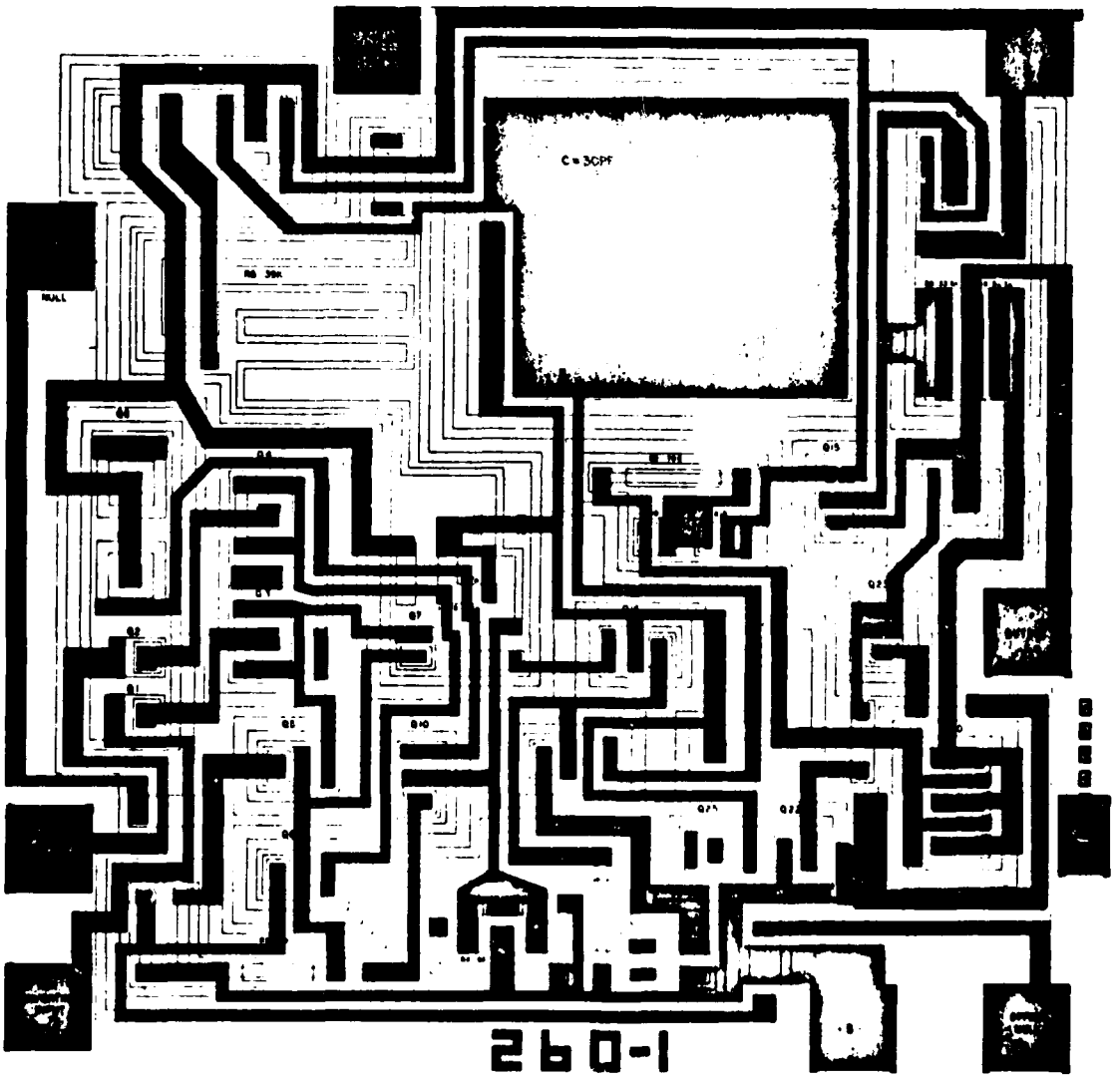


Figure 3 741 Operational Amplifier Topological Composite

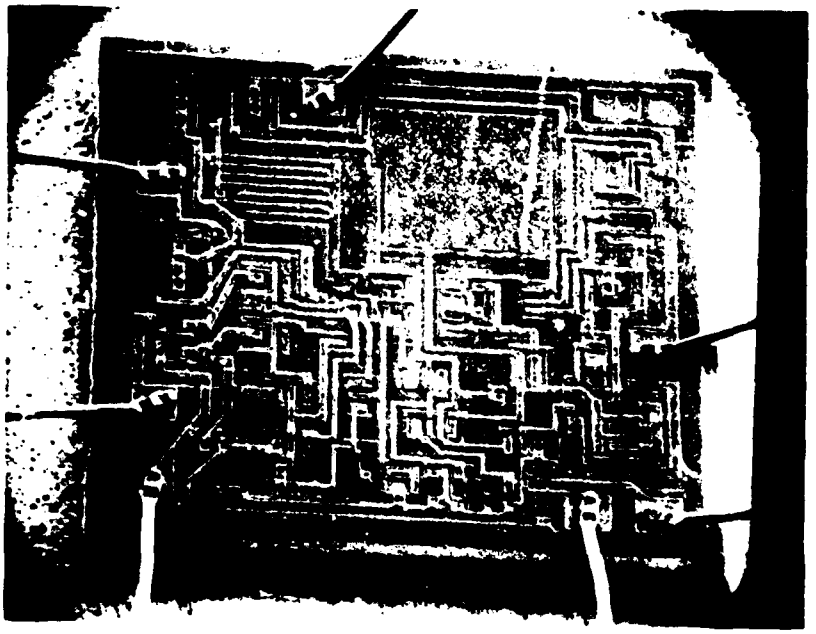


Figure 4 741 Operational Amplifier Topological Photograph

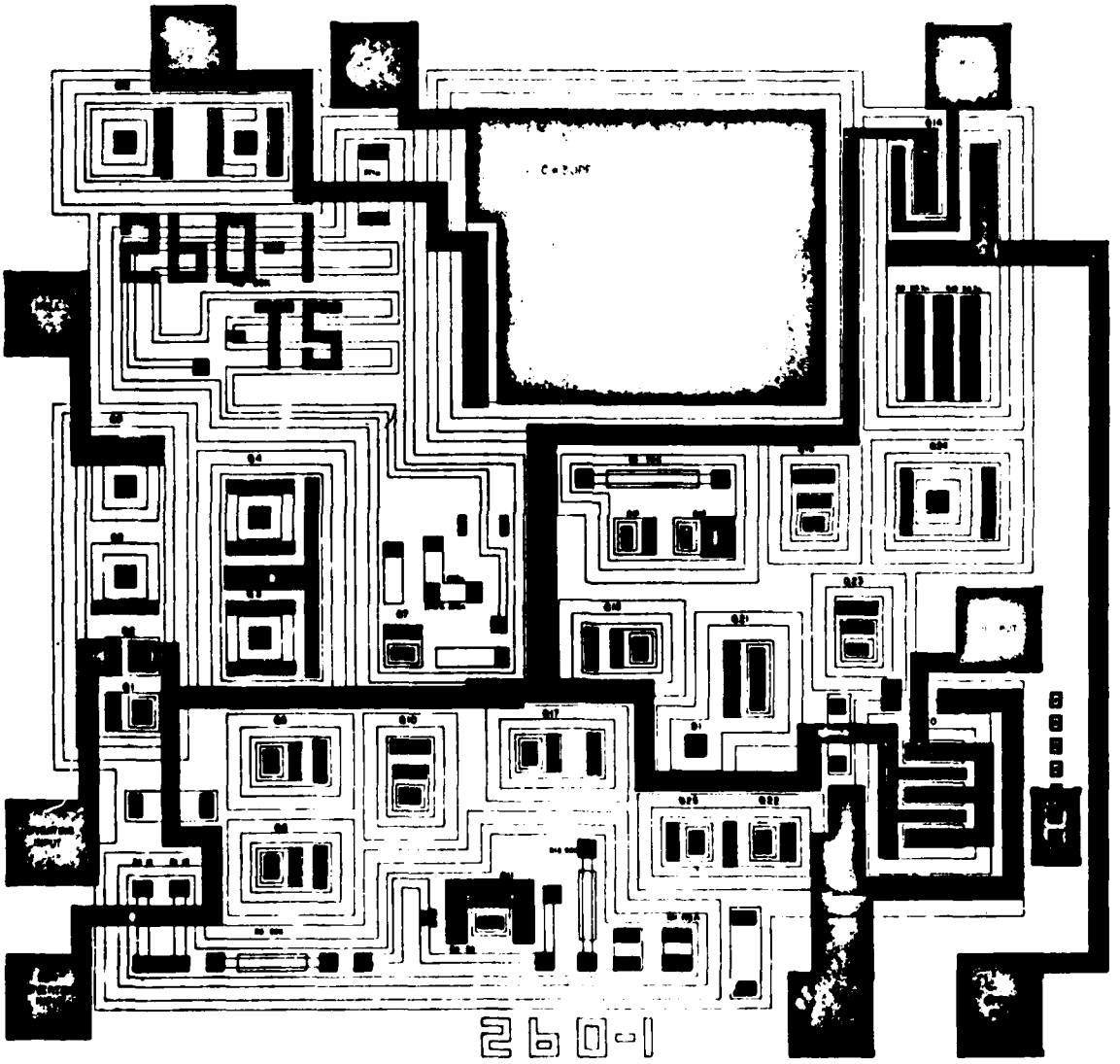


Figure 5 Test Element Group Topological Composite

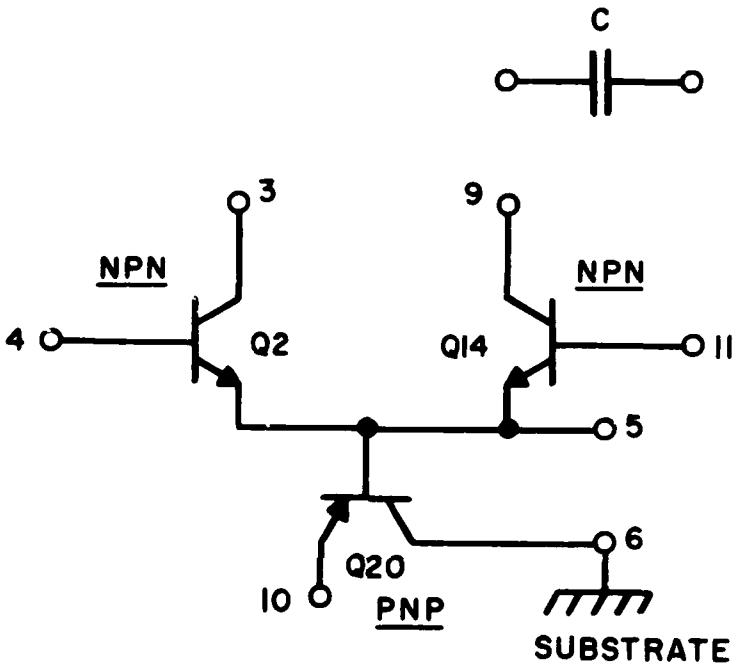


Figure 6 Test Element Group Schematic

D. ASSEMBLY AND PACKAGING TECHNOLOGY

The latest state-of-the-art assembly processing and packaging technologies available were utilized in the devices for the fulfillment of this program. In general, there were three types of package assemblies used:

- Hermetic ceramic 14 lead dual-in-line package, with standard aluminum chip metalization and ultrasonic bonded Au or Al lead wires,
- Plastic encapsulated 14 lead dual-in-line package, with standard aluminum chip metalization and thermocompression ball bonded gold lead wires,
- Plastic encapsulated 14 lead dual-in-line package, incorporating state-of-the-art assembly and processing features such as Silox overglass, gold bonding pads, wire sawed chip separation, gang bonded connections to the chip, a simultaneous reflow/welding of the fan-out pattern to the lead frame and an epoxy barrier encapsulating the chip. This resulted in an encapsulated device which was then transfer molded on a conventional lead frame.

The gangbond metalization technology will be described first, followed by the other assembly techniques. A general discussion of the advantages of the several packaging technologies is also included.

1. Gangbond Metalization

As envisioned, the gangbond technique involved developing a simple, low cost metalization technique to put adherent, plague-free solderable contact pads on conventionally processed, aluminized wafers. In this way, circuit wafers could be processed through wafer

test and inventoried before a decision need be made as to whether to commit that circuit wafer to conventional aluminum pad and wire bonding manufacturing lines, or to the new assembly process.

Five additional requirements, or needs were set for the gang-bond system. It should (1) be useful for automatic (gang bonding) assembly in the existing integrated circuit (copper lead frame) plastic packages; (2) be capable of producing chips which could be soldered to circuits on ceramic substrates or high temperature plastic films; (3) be capable of fabricating lead connections small enough to bond to chips yet large enough to be directly connected to printed circuit boards by soldering processes; (4) be capable of high bonding yields when applied to MSI or LSI chips having many contact pads (up to 100); and (5) be capable of allowing a chip to be soldered directly to metal or metalized ceramic heat sinks.

A specific fact to be emphasized, is that the assembly process had to be capable of directly soldering chips to high power dissipation copper lead frames as well as to conventional low conductivity materials such as kovar, nickel, nickel-iron, etc. This fact, as well as item (3) above, suggested a move away from aluminum leads, since they are difficult to solder and tend to electrolyze in the presence of humidity, copper, and some useful plastics.

The goals listed above were met, both by the chip metalization process, and the assembly system. Briefly, the system is based on:

- Gold contact pads,
- Tin plated, photoetched copper fanout-lead-patterns,
- Gold/tin impulse soldering cycle,
- Simultaneous bonding of all photoetched leads to the chip

and then to the lead frame,

- Use of a sprocketed plastic (35 mm) film to precisely index leads between operations,
- Reel-to-reel plastic film transport, handling equipment, and processes,
- Automatic indexing of separated chips (having their original x-y location) beneath a bonding tip,
- Automatic indexing of lead patterns, on film, between chips, and bonding tip,
- Total bonding cycle of 3 seconds.

Cycle time includes final alignment of chip to leads, bonding tip placement, heat cycle, cool cycle, tip removal and indexing to the next chip.

a. Wafer Preparation

The wafer preparation utilized standard IC bipolar processing through aluminum evaporation, masking and etching of contacts and conductors on top of the chip. At this point, wafers could be tested prior to being committed to an assembly technique.

The IC wafers selected for gangbond assembly underwent additional processing to put solderable gold-pads on the chips: First, the wafers were coated with glass in order to cover the aluminum conductor runs with a tough, protective insulating layer and mask. Next, the contact holes were etched through the glass to the aluminum contacts. Finally, the gold solder bumps, evaporations, photoresist and etching steps were completed. The resultant chip-pad or bump-contact structure is shown in the drawing of Figure 7.

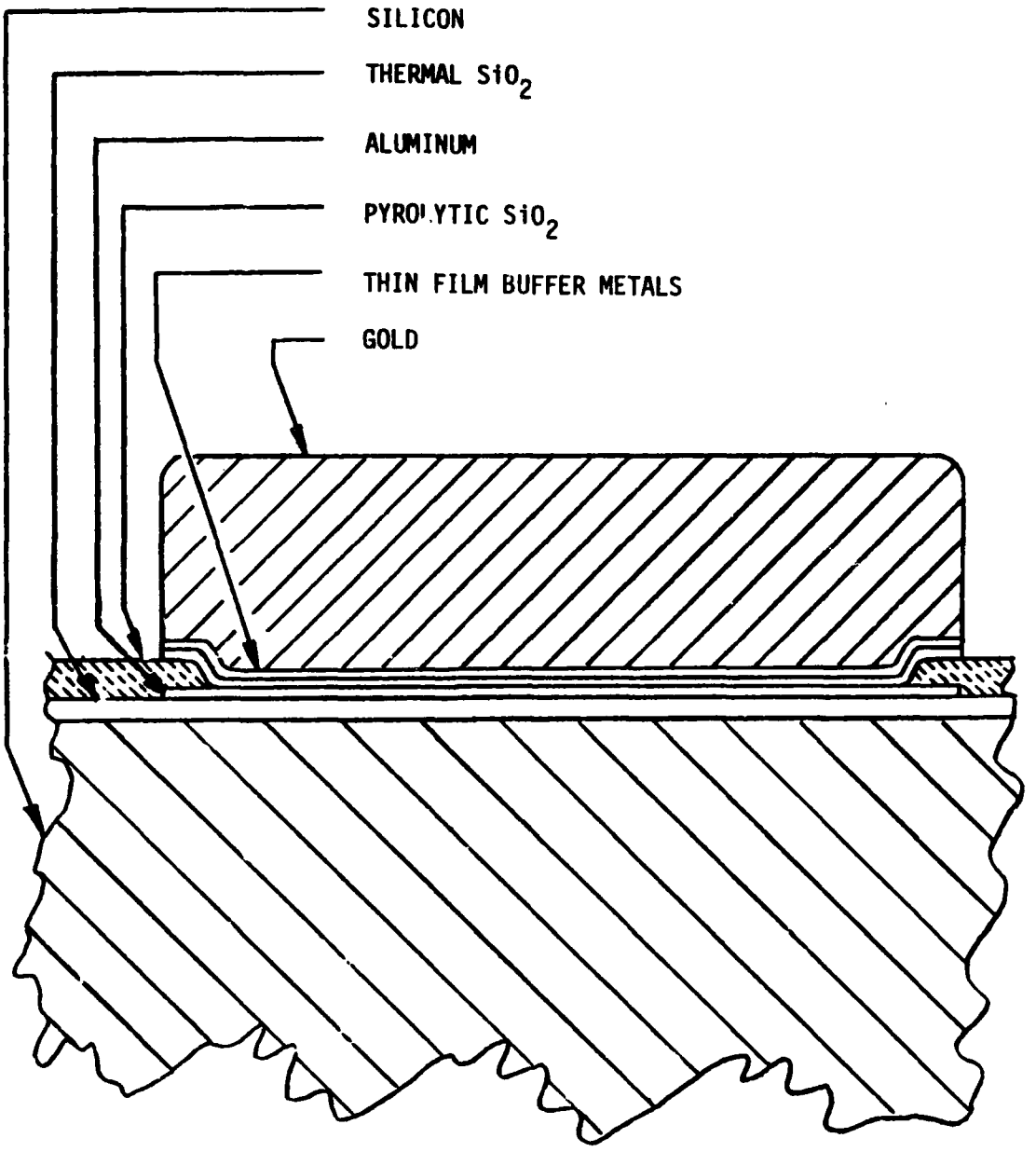


Figure 7 Gangbond Contact Pad Metalization

The wafers were then mounted onto a holder (nest-plate) with the gold bumps up, and wire sawed apart. After the chips were sawed apart the nest plate was cleaned (chips were retained in place) and the wafer of individual precisely located chips was then processed in the bonding machine. This chip bonder used the known chip-orientation to automatically and precisely present new chips to the bonding tip as required in the bonding cycle.

b. Gangbond Assembly Process

In the gangbond system, the conventional fly-wirebonding was replaced. The leads connecting the integrated circuit chip to the external lead frame were formed from a tin plated, laminated, copper foil (1.4 mil thick) photoetched to match the dimensions of the chip on the inside and to match the heavy copper lead-frame on the outside. The plastic film was a high temperature polyimide film, which served as a supporting and transporting medium in the assembly system. The use of reels greatly simplified handling, processing, and transport problems from station to station in the assembly area.

A machine was developed to facilitate "lead to chip" bonding, featuring reel-to-reel handling of chips and leads. This machine is capable of bonding all the leads to a chip in one operation, and indexing to a new chip and new lead pattern for the next cycle in a total cycle time of less than 3 seconds.

A production tool was also developed to cut out individual plastic-supported lead-patterns (with chips on them). In addition, this machine welded all the outer ends of the lead patterns in one operation to the standard copper lead frame used in one type of

the plastic dual-in-line, DIP package.

2. Package Assembly

The hermetic ceramic dual-in-line package used by one manufacturer contained a chip with standard aluminum metalization which was separated by conventional scribe and break techniques. The chip was mounted to the ceramic header using no preform. Gold wires were then ultrasonically bonded to the chip. A conventional sealing technique was used in which a Kovar lid was brazed to the ceramic header with a preform. The process flow is shown in Figure 8.

The 14 lead plastic DIP contains a chip with standard aluminum metalization which was separated by conventional scribe and break techniques. The chip was eutectic mounted to a silver plated copper lead frame using a preform, and gold wires were then thermocompression ball bonded to the chip. A silicone barrier was applied to the chip by spraying. The devices were then loaded into a mold on lead frames of five unit lengths each. An epoxy was used for the encapsulant. A two hour cure followed the molding, as shown in the process flow illustrated in Figure 9.

The 14 lead DIP gang bonded assembly techniques contained a chip with 12,000 angstroms of normal thermal oxide. Then 12,000 angstroms of silox glass were deposited on the thermal oxide and the metalization. Following the deposition of the glass vias were opened up to expose the aluminum pads. A thin flash of buffer metal was then deposited over the whole wafer to allow conductivity for gold electroplating. Using conventional photolithographic techniques, the wafer was then masked with photoresist except in

CERAMIC PACKAGE

14 LEAD DUAL-IN-LINE PROCESS FLOW

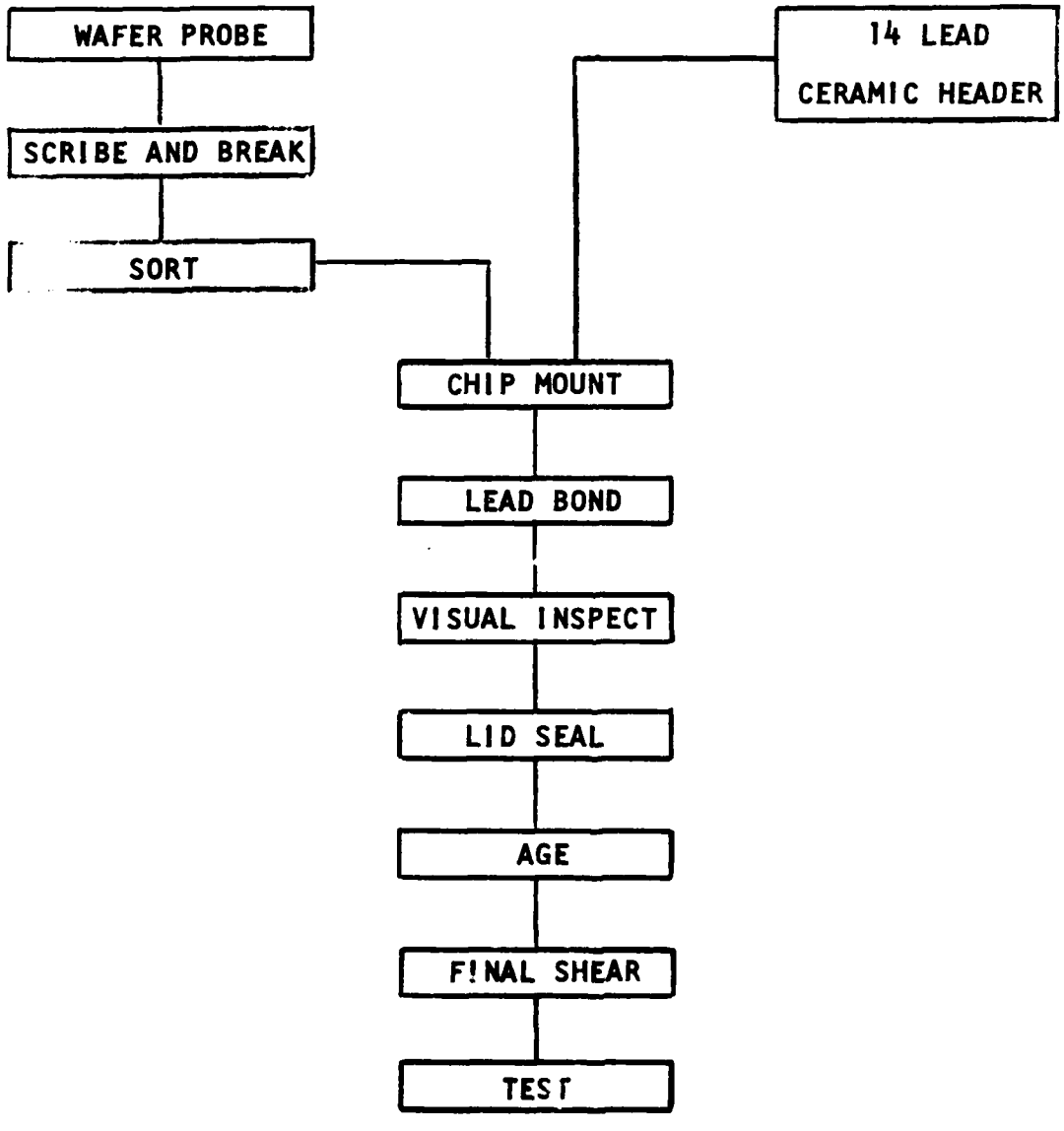


Figure 8 Ceramic DIP Assembly Process Flow

STANDARD PLASTIC ENCAPSULATED PACKAGE

14 LEAD DUAL-IN-LINE PROCESS FLOW

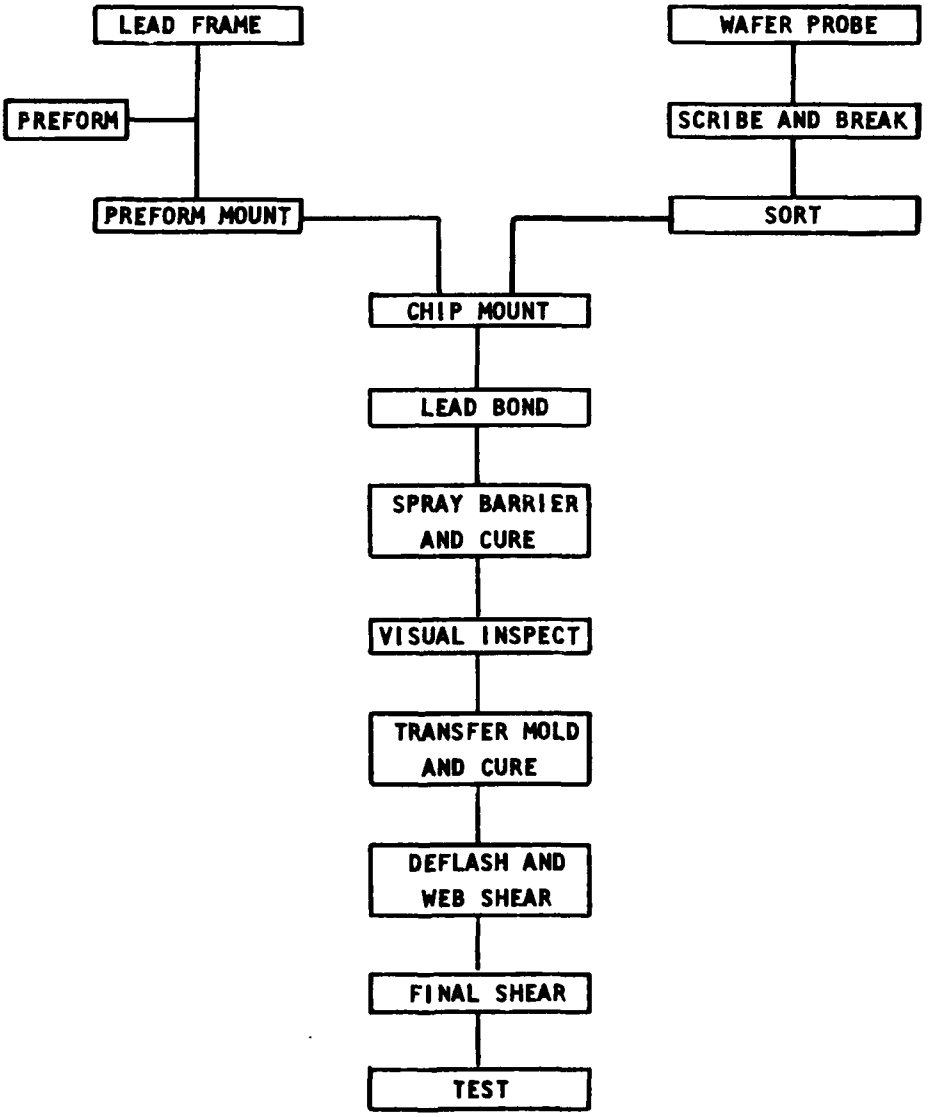


Figure 9 Plastic Encapsulated DIP Assembly Process Flow

the pad areas, which are gold plated. The photoresist was removed and the buffer metal etched off, with the gold pads acting as a mask for the pad areas. During this etch step, any aluminum exposed such as by pinholes is passivated by a special additive to the etch. Finally the wafer was mounted on a plastic nest-plate prior to wire sawing. The wafers are wire sawed and are now ready to be processed in the gang bonder for simultaneous bonding of all of the pads on each chip to the tin plated copper fan out pattern. The process flow is shown in Figure 10.

The gangbond leads are an etched electrodeposited copper foil laminated to a polyimide plastic 35 mm punched strip. The lead configuration is such that they will line up with the gold pads on the chip. The wire sawed wafer mounted to the nest plate was aligned in the highly mechanized bonder and a heated bonding tip simultaneously bonded all of the leads to their respective pads on the chip forming a gold-tin eutectic. The film and nest plate were then rapidly indexed to present the next set of inner lead fingers to the next chip for bonding.

The completed strip of inner lead bonded assemblies was loaded onto the outer lead bonder for separation of the lead pattern from its polyimide carrier strip (Item V Figure 11c) and welding it to a tin plated copper DIP lead frame (Item VI Figure 11c). Once set up, this operation was done automatically, with an operator in attendance to prevent any visual rejects from being welded to the lead frame.

The devices attached to the copper lead frame then were processed through an epoxy dispensing station which dispensed epoxy in such a manner as to completely surround the chip. The epoxy was then cured.

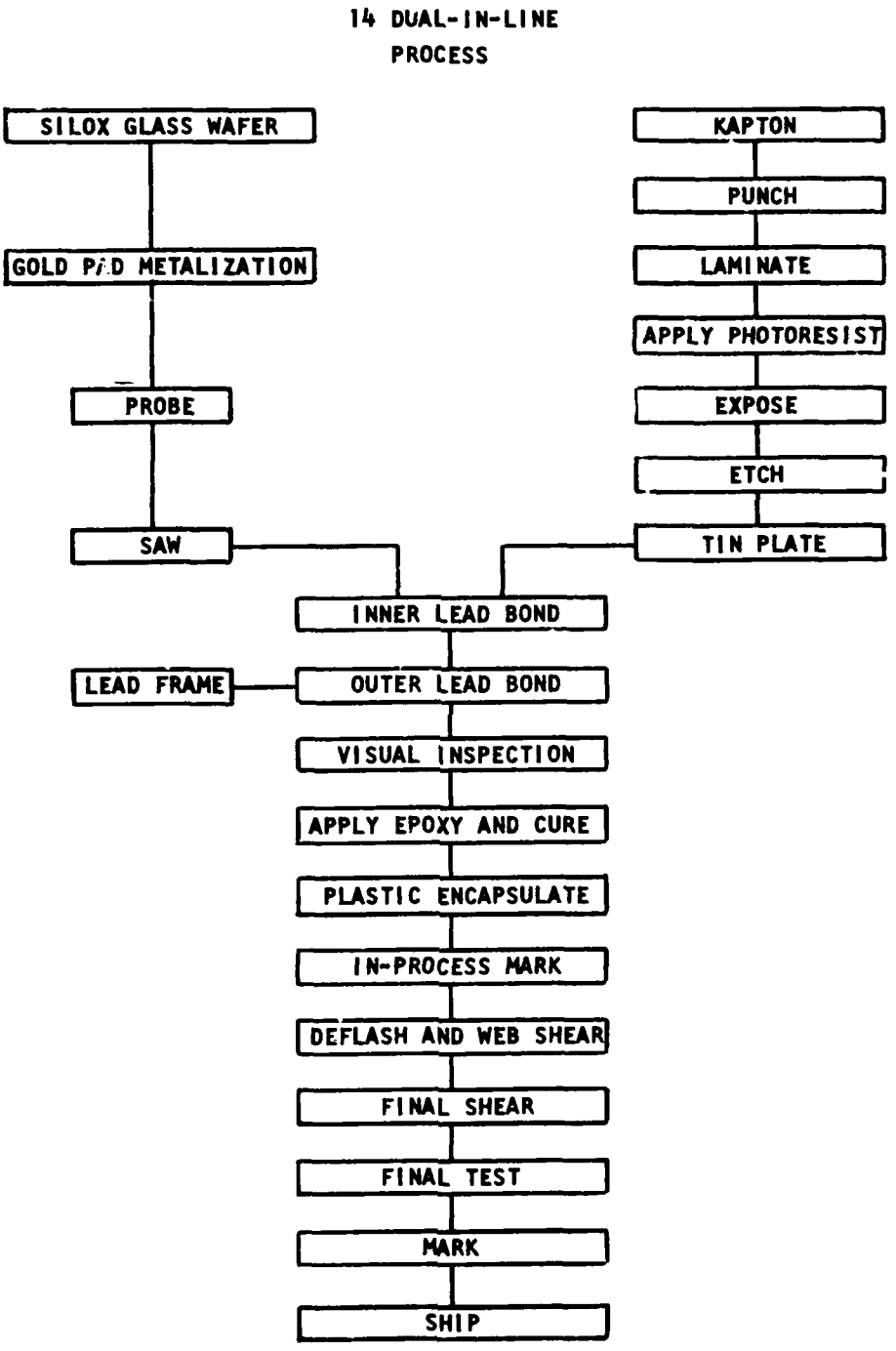
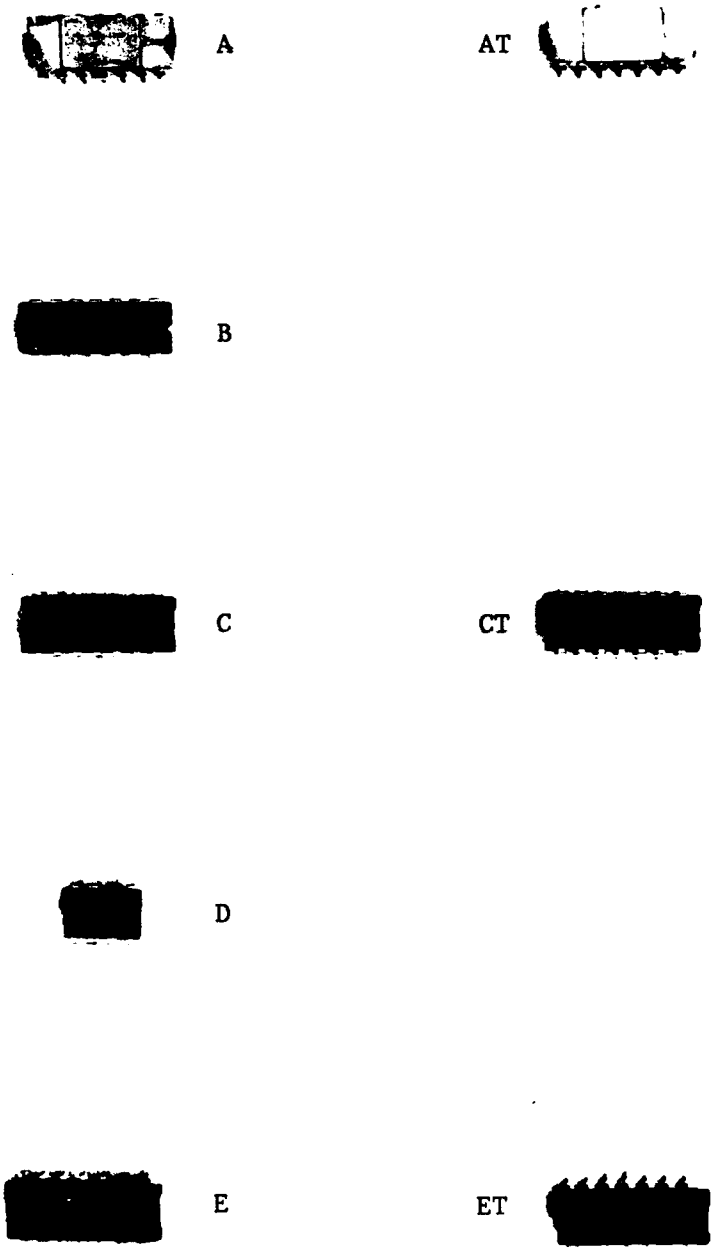
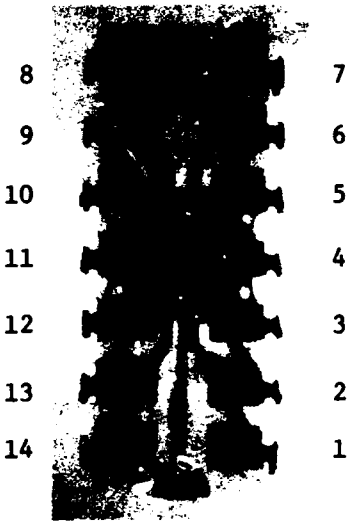


Figure 10 DIP Gangbond Assembly Process Flow

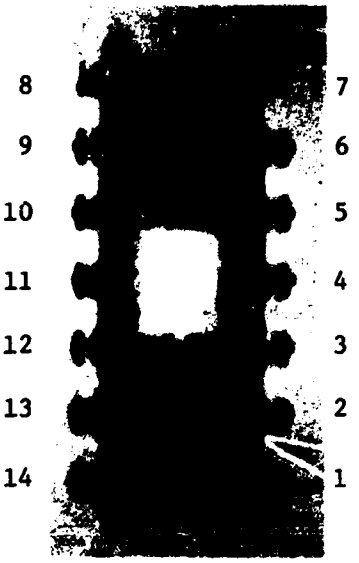


Photograph of Program Vehicle Packages

Figure 11a 741 Photographs, X-ray Views and Gangbond Exploded View (Continued)

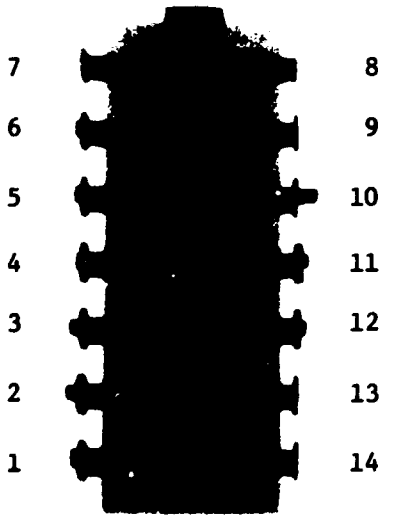


A, AT Ceramic Package



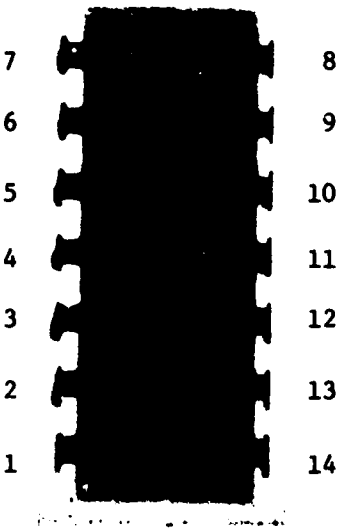
B Ceramic Package

Non-uniformity in Thickness of the Dense Lead Glass Used to Seal the Package Results in Xray Pattern Non-uniformity. Aluminum Internal Wires are Transparent to Xray.



C, CT Epoxy Package

D Silicone Package



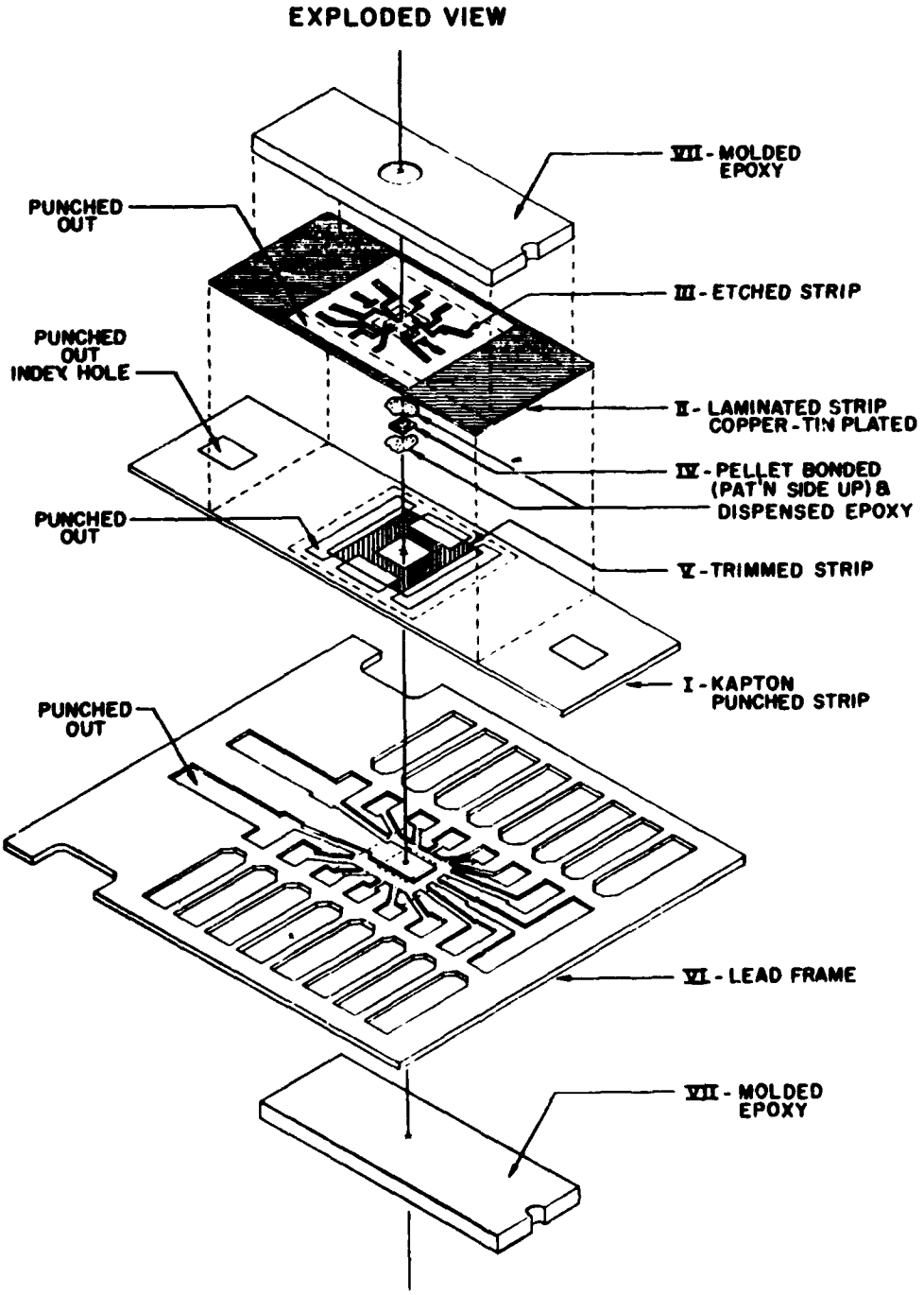
E, ET Epoxy Package

Pins 3, 4, 5, 6, 9, 10, 11 were Utilized for Circuit Connections

X-rays of Lead Frames on Program Vehicles, 3.7X Magnification

Figure 11b 741 Photographs, X-ray Views and Gangbond Exploded View (Continued)

PLASTIC 14 LEAD DUAL-IN-LINE ASSEMBLY



Gangbond Exploded View

Figure 11C 741 Photographs, X-ray Views and Gangbond Exploded View (Concluded)

Devices were next loaded into the mold on lead frames of 5 unit lengths each. An epoxy was used in this transfer molding process, (see Item VII Figure 11). It should be noted that all three types of the first manufacturers device assemblies were visually inspected prior to encapsulation.

3. Technical Discussion: Gangbond Assembled Plastic Encapsulated DIP

a. Chip Sealing

The silox overglass on these plastic encapsulated units offered additional dielectric protection over and above the normal thermally grown oxide and consequently reduced the possibility of surface inversion due to any ionic contamination. Furthermore, since all of the aluminum contacts and connectors were covered with overglass, and the aluminum pads were covered with gold, there should be resistance to aluminum metalization corrosion. In addition, still another protective barrier was applied in the form of epoxy encapsulation of the chip prior to transfer molding. This dual encapsulation offered superior resistance to moisture penetration, thermal shock and temperature cycling due to the characteristics of cast epoxy compared to those of transfer molded epoxy.

b. Wire Sawing

Wire sawing has several compensating advantages over scribing, in spite of the additional silicon required for the kerf loss from the saw cut. First of all, wire sawing used a very fine abrasive grit which produced a minimum of edge and structural damage to the silicon. It eliminated incipient edge cracks that could develop during conventional scribe and break. These cracks could

propagate further during subsequent stressing of the device. In addition, chips were never abraded against each other since they retained their original wafer position on the nest plate until they were bonded to the lead pattern. The last feature is that by maintaining this true position of one chip with respect to the other, as in the original wafer, it was possible to use an X-Y table to precisely index each chip into position for lead bonding.

c. Gangbond Inner Lead Connections

One of the problems encountered in molding of flying wire devices was the shorting or near shorting of leads to the chip edge or frame due to disruption of the lead dressing with the flow of the plastic material into the mold cavity. The gangbond fan out pattern from the chip to the lead frame was essentially rigid and would not deflect during molding. An additional feature was that wire sawing made it possible to leave glass in the streets so that the leads were prevented from edge shorting to the chip. Contrary to typical pull strengths of 13 to 14 gms on 1.5 mil diameter wire, TCB or ball bonded, gangbond strengths were typically 30 gms.

d. Plastic Encapsulation

In the particular assembly/encapsulation system used, it is of particular interest that the linear coefficient of expansion of the copper lead frame was closer to that of the epoxy encapsulant than conventional Kovar frames. Another salient feature of this system was that the chip was not attached to the lead frame and was free-floating in the inner encapsulant and therefore was not subjected to the expansion and contraction mismatches between

the lead frame and the encapsulant.

In summary, the latest technologies available have been incoporated in the gang bonded assembled plastic dual-in-line package. These included:

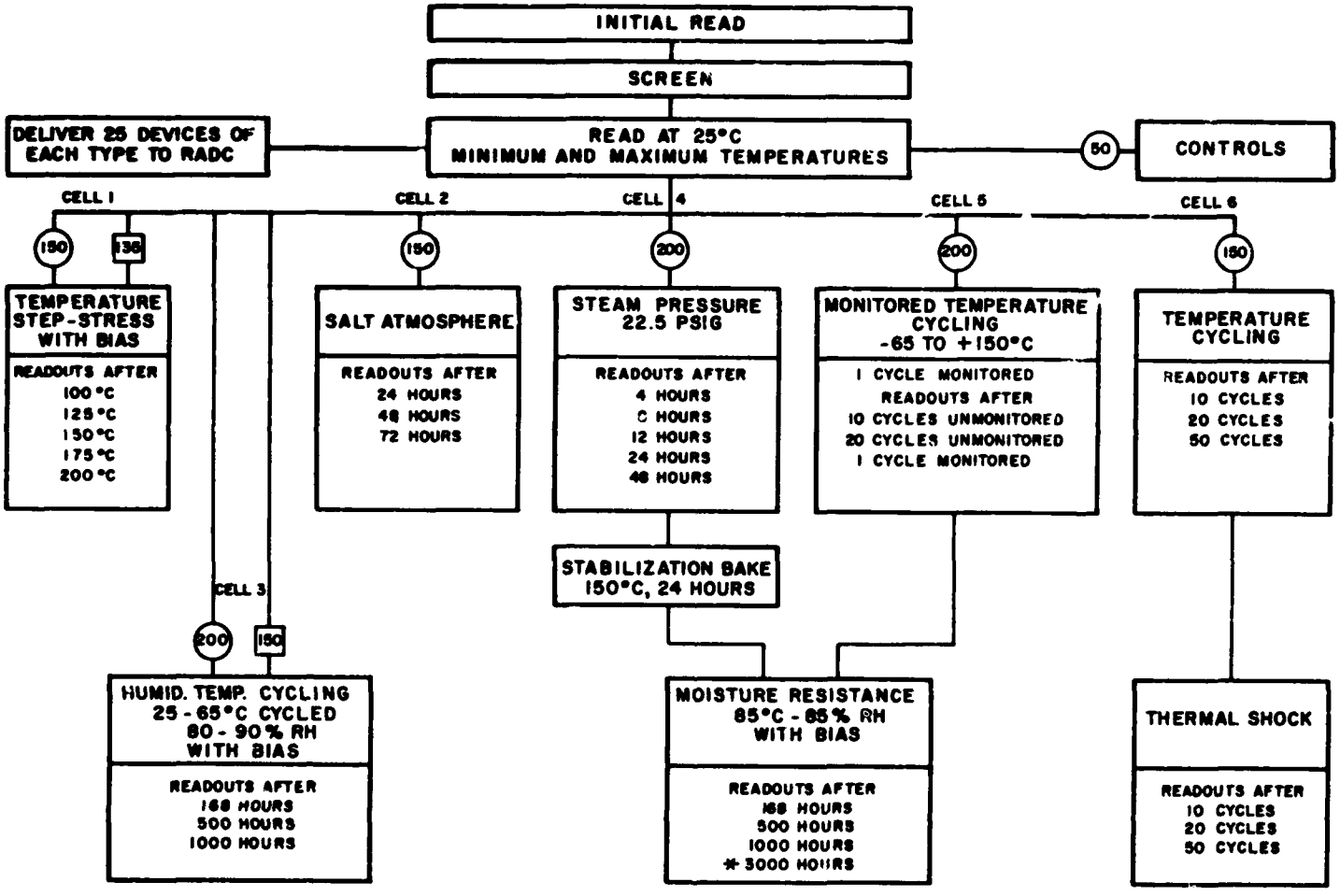
- Greater integrity of inner lead bonds,
- Greater lead strength,
- Gang welded outer leads to lead frame,
- Glass sealed chip,
- Wire sawed chip,
- Dual encapsulation,
- Copper lead frame (closer match to epoxy),
- Free floating chip.

SECTION III

TEST PLAN

A comprehensive reliability evaluation program has been designed for linear microcircuits fabricated in ceramic and plastic packages. The selection of the vehicles for the designed stress measurement program afforded a broad and comprehensive coverage of current state-of-the-art production devices. The program was designed to determine the basic failure mechanisms associated with the different fabrication and processing methods and materials of the chip structure, the lead bonding and the encapsulation. The evaluation program was directed toward determining the relative suitabilities of representative, production, linear microcircuits for military and industrial qualification. The emphasis of the stress program has been on ascertaining the resistance capabilities of ceramic and plastic encapsulated structures to high temperature - humidity environments with bias applied. A much needed re-examination of the response of hermetic integrated circuit packages to such stressing was obtained in conjunction with the plastic package evaluation.

The linear microcircuit reliability evaluation program is shown in Figure 12. The six major stresses used are identified by a cell number which was utilized throughout the program. The test matrix was statistically designed for valid performance comparisons of ceramic and plastic encapsulated structures. In addition, valid comparisons were made of chips with different materials and processing encapsulated within the same plastic packages. This was



TOTAL SAMPLE SIZE BALANCED OVER 5 OPERATIONAL AMPLIFIER VEHICLES SHOWN ENCIRCLED.

TOTAL SAMPLE SIZE BALANCED OVER 3 TEG VEHICLES SHOWN IN SQUARES.

* DEVICES FROM CELL 4 WERE STRESSED 3,000 HOURS.
DEVICES FROM CELL 5 WERE STRESSED 2,000 HOURS.

Figure 12 Test Plan

done with a minimum confounding with other variables - namely, different manufacturers, different chip circuit designs and lot-to-lot heterogeneity. The chips for three of the different vehicles were processed through identical wafer diffusion, photoresist and etching steps. Two of the three vehicles contained chips derived from wafers processed through the same diffusion and metalization steps and differ only in the final encapsulation - ceramic versus plastic. The other vehicle consists of the same source chips with additional processing steps. These steps included gangbond metalization, a pyrolytically deposited glass on the chip surface and a new automatic bonding system with planar leads. Chips balanced within a wafer lot were fabricated into the three vehicle types. Lot identity was maintained for device traceability.

Stress data was also obtained from packaged TEG structures for those devices manufactured by one supplier. The alternative to testing large numbers of monolithic ICs is that of packaging and stress testing of TEGs. These structures are derived from the same wafers containing the identical geometry and processing steps as the microcircuit chips and would exhibit the same reliability characteristics. The TEGs are conductor patterned so that measurement and stressing of some element parameters are possible resulting in a much more thorough reliability and failure analysis evaluation than can be accomplished on a complex linear circuit. In a previous reliability program involving monolithic digital and linear integrated circuits, the TEG was positively demonstrated as a key instrument in predicting circuit characteristics and stress performance.

In order to trace the history of devices through the various

applied stresses for the five vehicle types, all program test vehicles were adequately serialized.[1] All specified circuit and TPC element parameters were measured before and after stress at the scheduled readouts indicated in the program plan. The selected characteristics to be monitored before and after stress were chosen to be those that were most sensitive to the effects of moisture, surface contamination, intermittency and resistance change in the lead bond-metalization system. The characteristics and limits are shown in Figure 13 which also contains the Teradyne test number and end-of-life (EOL) or degradation limits. The parameters with EOL limits were the critical ones used for the interim and final readouts during the program.

Replicated circuits per vehicle for each of the five vehicles were randomly assigned to the different stresses, as indicated in Figure 12, affording a repeatability measure of performance for the same vehicle within a stress as well as the relative reliability performance between the different vehicles. Reference to the program plan also shows sequential stressing where devices assigned to temperature cycling and pressure cooker were subsequently subjected to the long term temperature-humidity-bias stress. Thus, for those units subjected to steam pressure followed with a recovery bake, a unit-to-unit correlation is afforded between the short term accelerated temperature-humidity stressing and the long term milder temperature-humidity stressing. An assessment was also made of the degrading effect of temperature cycle stress preceeding long term moisture resistance. Methods for lot qualification and short term evaluation of process and design differences may be based upon these results, and suggestions for these usages are discussed in the conclusions section of this report.

1. A four digit number is used for device identification. The first digit is the Cell number and the last three digits identify the device.

PARAMETER	SYMBOL	TEST	CONDITIONS	INITIAL LIMITS +25°C		OBJECTIVE LIMITS TEMPERATURE -55°C°		TEMPERATURE +125°C		EOL +25°C		UNITS	
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
OUTPUT VOLTAGE SWING	V_{OPP+}	1	R_L = 2K	10		10		10				V	
OUTPUT VOLTAGE SWING	V_{OPP-}	2	R_L = 2K	10		10		10				V	
POWER SUPPLY CURRENT DRAIN	I_{PS}	5			2.8		3.3		2.5		±0.56	mA	
INPUT BIAS CURRENT	I_{IB}	6			500		1500		500		±150	nA	
INPUT OFFSET CURRENT	I_{IO}	7			200		500		200		±40	nA	
COMMON MODE REJECTION RATIO	CMRR	10	$R_S \leq$ 10K		7.4		7.4		7.4			mV	*
INPUT OFFSET VOLTAGE	V_{IO}	20	$R_S \leq$ 10K		5.0		6.0		6.0		±1.0	mV	*
LARGE SIGNAL VOLTAGE GAIN	$A_{VS(\pm)}$	21	R_L = 2K, V_{OUT} = ±10V		400		800		800			μV	*
POWER SUPPLY REJECTION RATIO	PSRR	24	$R_S \leq$ 10K		1.8		1.8		1.8			mV	
OFFSET VOLTAGE ADJUSTMENT RANGE	$V_{IO(ADJ)+}$	25		6.3								mV	
OFFSET VOLTAGE ADJUSTMENT RANGE	$V_{IO(ADJ)-}$	26		6.3								mV	
INPUT VOLTAGE RANGE	V_{IPP-}	12			10		10		10			(μA)	*
INPUT VOLTAGE RANGE	V_{IPP+}	13			10		10		10			(μA)	*

*NOTE: These parameters are measured indirectly and the units shown are correct for the measurement made. A calculation is necessary to convert to the normal units.

Figure 13 Monitored Electrical Characteristics and Limits

The test program was conducted on screened parts in general accordance with MIL-STD-883, Class C, (see Figure 14) so that the long term basic failure mechanisms associated with linear microcircuit devices can be uncovered and analyzed. The internal visual (precap) inspection was performed (in general accordance with Method 2010) on those devices manufactured by one source. All of the devices were temperature cycled and measured electrically.

The stress procedures involved step-stressing, combination and sequential stressing and extended stress-in-time testing. Results from the stress program were used to determine the relative susceptibilities of the different vehicles to surface, metalization, bond and encapsulation failures.

Simultaneous stressing at temperature, humidity and bias, cycled and non-cycled, assessed the die passivation and sealing integrity as well as the resistance of the multi-lead package to moisture. Thus, accelerated salt atmosphere and steam pressure stressing, the long term cycled temperature-humidity-bias, THB, and the steady state temperature-humidity-bias assessed the relative degree and effect of moisture penetration of the seal and along the lead frames leading to effects on the internal metalization. Further, the cycled THB stressing assessed the incidence of electrochemical corrosion of the external lead frame. The tendency toward conductive bridging between leads under a humid environment and electric field can lead to internal pin-to-pin shorts.

The temperature stress with applied bias was used to induce internal surface effects. This type of stress assessed the contamination of ionizable content of the encapsulation material and

MIL-STD-883 TEST METHOD AND REQUIREMENT

SCREEN	CLASS C
INTERNAL VISUAL (PRECAP) 1/	2010 TEST CONDITION B
STABILIZATION BAKE	1008 24 HOURS, MIN. TEST CONDITION C (150 ± 25°C)
TEMPERATURE CYCLING	1010 TEST CONDITION C
FINAL ELECTRICAL TESTS	a. STATIC TESTS 1. AT 25°C 2. AT MAX., MIN. OPERATING TEMPERATURE 2/
EXTERNAL VISUAL 3/	2009

1/ TO BE ACCOMPLISHED PRIOR TO ENCAPSULATION USING ALL APPLICABLE CRITERIA OF METHOD 2010.

2/ THIS TEST IS REQUIRED TO ESTABLISH CONTINUITY OF THE MICROCIRCUIT BONDS AND CONNECTIONS AT THE SPECIFIED TEMPERATURE EXTREMES. THEREFORE, THE DETAIL SPECIFICATION SHALL CONTAIN SUFFICIENT STATIC TESTS FOR SCREENING TO ESTABLISH CONTINUITY FROM ALL USED EXTERNAL LEADS TO THE DIE OR SUBSTRATE. AS AN ALTERNATIVE TO USE OF STATIC PARAMETER TESTS FOR THIS PURPOSE, A CONTINUITY TEST (THRESHOLD) PROGRAM WHICH ESTABLISHES CONTINUITY FROM ALL USED EXTERNAL LEADS TO THE INTERNAL MICROCIRCUIT ELEMENTS MAY BE EMPLOYED.

3/ UNLESS OTHERWISE SPECIFIED, THE EXTERNAL VISUAL INSPECTION NEED NOT INCLUDE MEASUREMENT OF PHYSICAL DIMENSIONS.

Figure 14 Integrated Circuit Screening

its accessibility to critical areas of the chip. The effect of the glassivation barrier in retarding ion migration resulting in inversion layers and electrical parameter degradation was also examined.

The temperature cycling and thermal shock stressing evaluated the relative degrees of thermo-mechanical failure modes. Thus, the extent and effect of thermal expansion mismatching of the system structures of the materials, interaction of encapsulant, lead frame and bonding wires under cycled temperature extremes was made. A monitored temperature cycle test was performed for detecting intermittents which are not revealed at room temperature but may appear as opens at temperature extremes. This may occur, for example, with the force of the transfer molding process of plastic encapsulated devices with a flying lead bond system. The thermal shock stress is an accelerated test for inducing catastrophics due to weak bonds or thermal mismatch between the encapsulant and metal elements of the microcircuit. The intent of the stress program was to induce device response and it was planned to conduct physics of failure analyses on samples of degraded or failed devices.

The implementation of the program plan has included valid processing and assembly procedures with representative and adequate sampling of the lots in order to avoid misleading and erroneous conclusions. The test program included the elements of balance, randomization and replication so that a valid and precise component assessment of uniformity, reproducibility and stability could be made. R ndomization makes it possible to eliminate or control extraneous or nuisance variables such as operator, machine and lot differences. Randomization and balance insures that such extraneous variables are not confused or confounded with main stress or process

variables. Statistical planning also allows the handling of several factors simultaneously and can assess interactions between variables. This program design contained replicate lots of material for a given process, manufactured over a given period of time to assure that the performance results obtained are repeatable and representative and not peculiar to one lot of production. Sample size per lot per stress was realistic and adequate to measure significant effects relative to experimental error such as sample size fluctuations and measurement error.

A measurement control group of unstressed integrated circuit and TEG structures was monitored along with the scheduled programmed measurements of stressed devices. A valid analysis of measurement data requires thorough and continual monitoring of equipment repeatability and accuracy. The repeatability measure for a measured parameter is usually obtained by performing an analysis of variance on the representative unstressed shelf storage units measured daily over a period of time. The repeatability measure corresponds to the square root of the mean square (i.e. variance) of day-to-day measurement variations and is necessary for determining what constitutes significant parameter degradation or failure attributed entirely to the particular stressing of the structure. Ascertaining the repeatability measure does not end the need for continual control of device measurements over the program period. Data from the control group was examined for any equipment anomalies, biases or drift variation or equipment-induced failures.

The electrical parameter measurements of the 741 operational amplifier were made on a Teradyne automatic test set. This is a high speed system which is capable of datalogging. A special test to

check the leakage currents between adjacent unused pins was performed on an automatic test set designed for discrete device parameter measurements. This test set was used to measure the leakage currents and beta of the TEG transistors.

It was recognized that the devices on the stress program would be inserted into and extracted from the test sockets many times during the course of the contract. This led to the possibility of damaging the device external leads. A test socket was located which uses a lever action to make contact and has a zero insertion and extraction force. The decision was made to use this socket on all of the special test fixtures for the environmental tests. The socket was also used with the TEG automatic test system. One problem developed at the higher temperatures (175°C and above). The top section of the socket warped under the lever force, which allowed the spring contacts to open. It was necessary to wedge the sockets closed to maintain electrical contact.

It will be noted that several of the stress cells shown in Figure 12 indicate that electrical bias was applied to the devices during the stress. Schematics of the bias circuits used for the operational amplifiers and the TEGs are shown in Figure 15. The circuits were designed to apply the largest practical voltage fields while keeping any internal dissipation at a minimum value. (About 30 mW for the 741.) This resulted in achieving approximate reverse bias configurations and avoided as much as possible the "drying out" of any moisture which had been driven into the device.

A special set of test equipment was utilized in this program to perform the Monitored Temperature Cycle (MTC) Test. The equipment consisted of a programmable temperature chamber, a Teradyne J259 computer controlled test system, an electronic

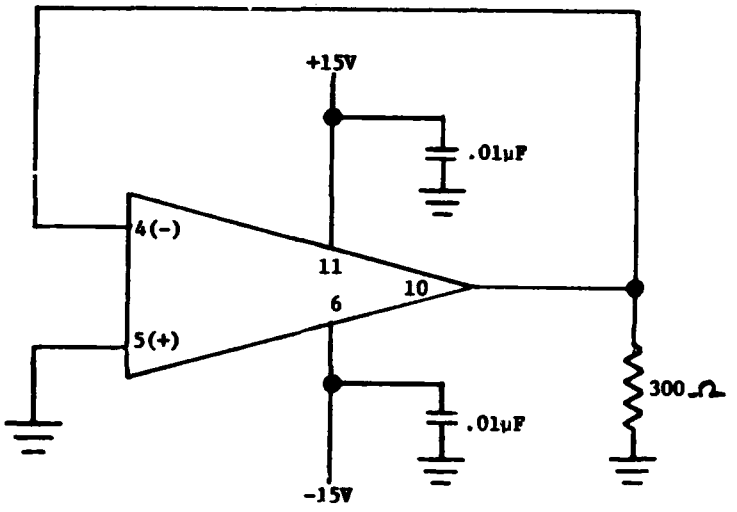


Figure 15a Operational Amplifier Bias Circuit

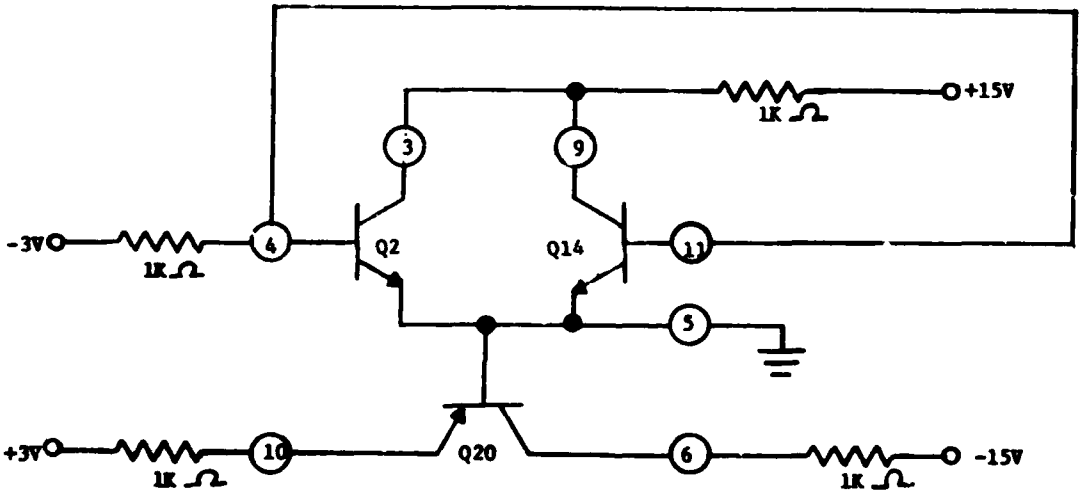


Figure 15b TEC Bias Circuit

thermometer, a device selection matrix, and readout equipment. A photograph of the equipment is shown in Figure 16a and a block diagram is included in Figure 17. A closer view of the chamber door, with the device sockets, is shown in Figure 16b. In operation, 40 devices at a time were loaded in the chamber which was then cycled from room temperature to +150°C back to room temperature and down to -65°C, then returned to room temperature. During the cycle, the six active pins of the operational amplifier were monitored (to the substrate) for intermittent opens. The programming and control circuitry was designed so that all 240 tests were made within each 2°C incremental change in temperature. The readout information identified the device card, socket and pin and the temperature at which the open occurred. If no opens were detected, the temperature of the chamber was recorded.

A flow chart of the MTC test is shown in Figure 18 which provides a detailed explanation of the MTC test. The temperature sensor used a calibrated silicon diode, heat sinked to provide some thermal lag, mounted in the chamber and connected to an electronic thermometer. The output to the test system for computer oven control was 10 mV/°C.

The forced current during test was 10 μA, in each case, to avoid welding an intermittent open contact back together. Because of the varying number of device junctions in the current flow path, three current sources were used. The sources all used a ramp voltage to force the current and the device was considered to have an open connection if the ramp voltage reached its preset limit.

Figure 16a Monitored Temperature Cycle Equipment

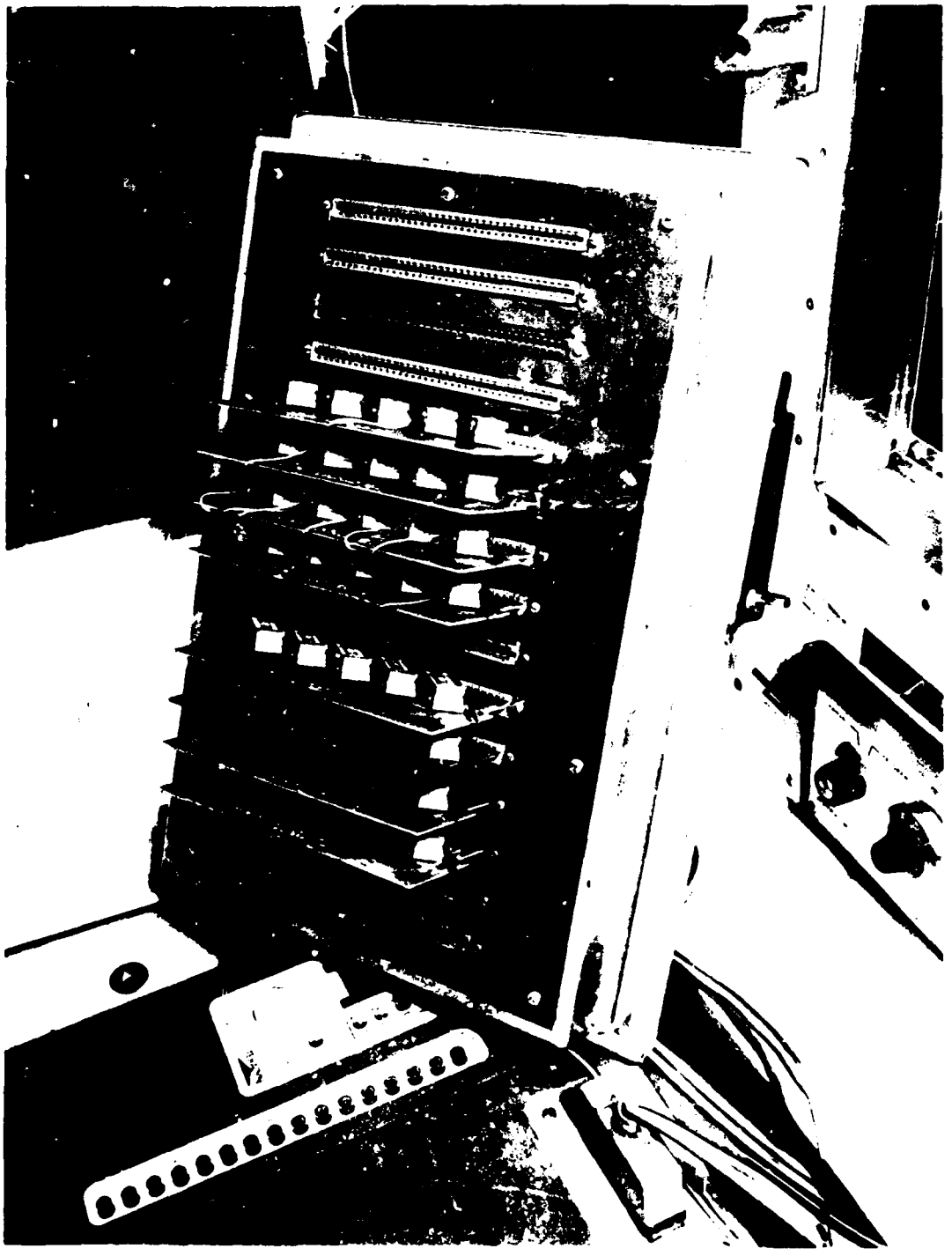


Figure 16b MTC Equipment Chamber Door

MTC EQUIPMENT BLOCK DIAGRAM

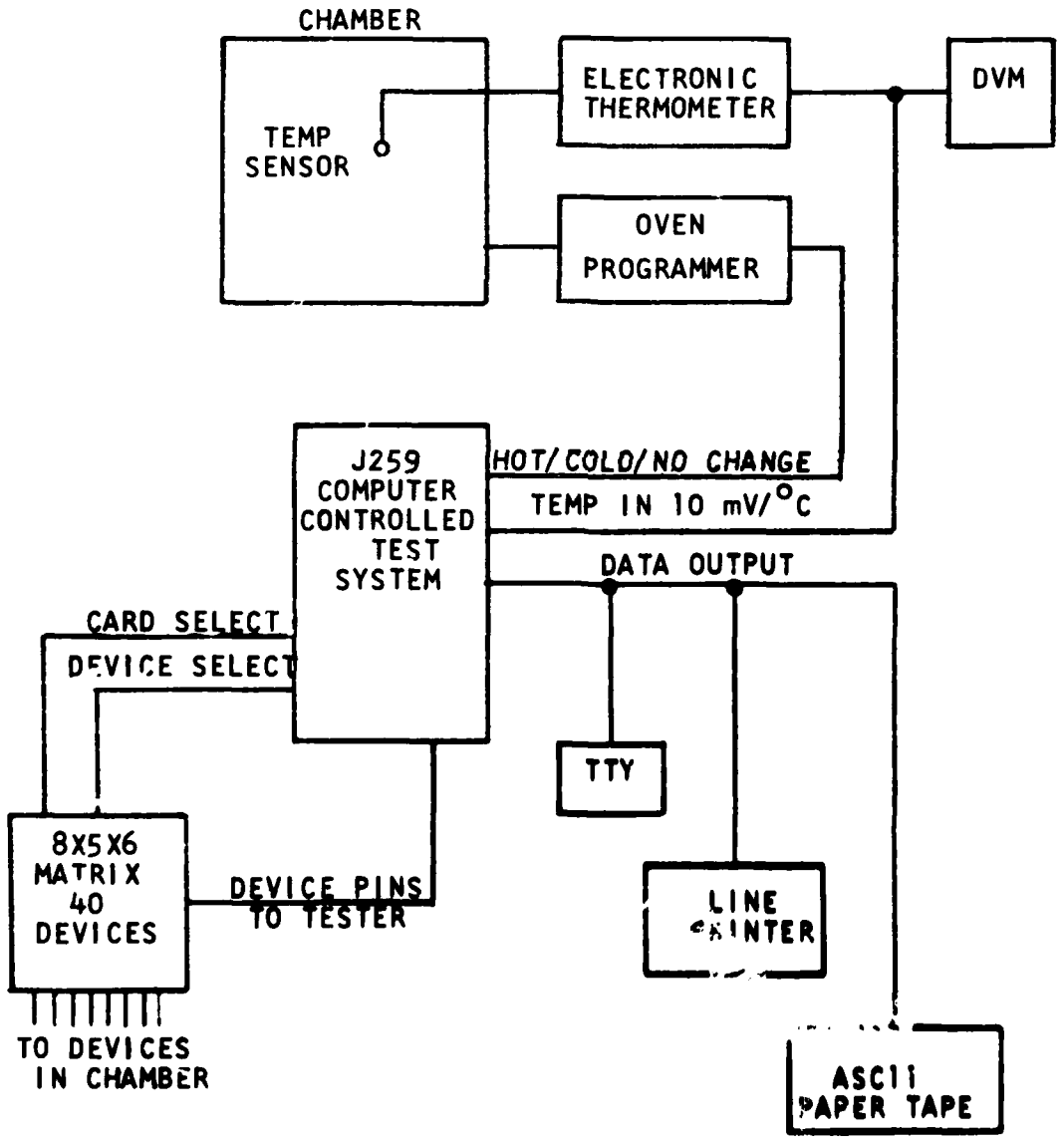


FIGURE 17 MONITORED TEMPERATURE CYCLE (MTC) EQUIPMENT

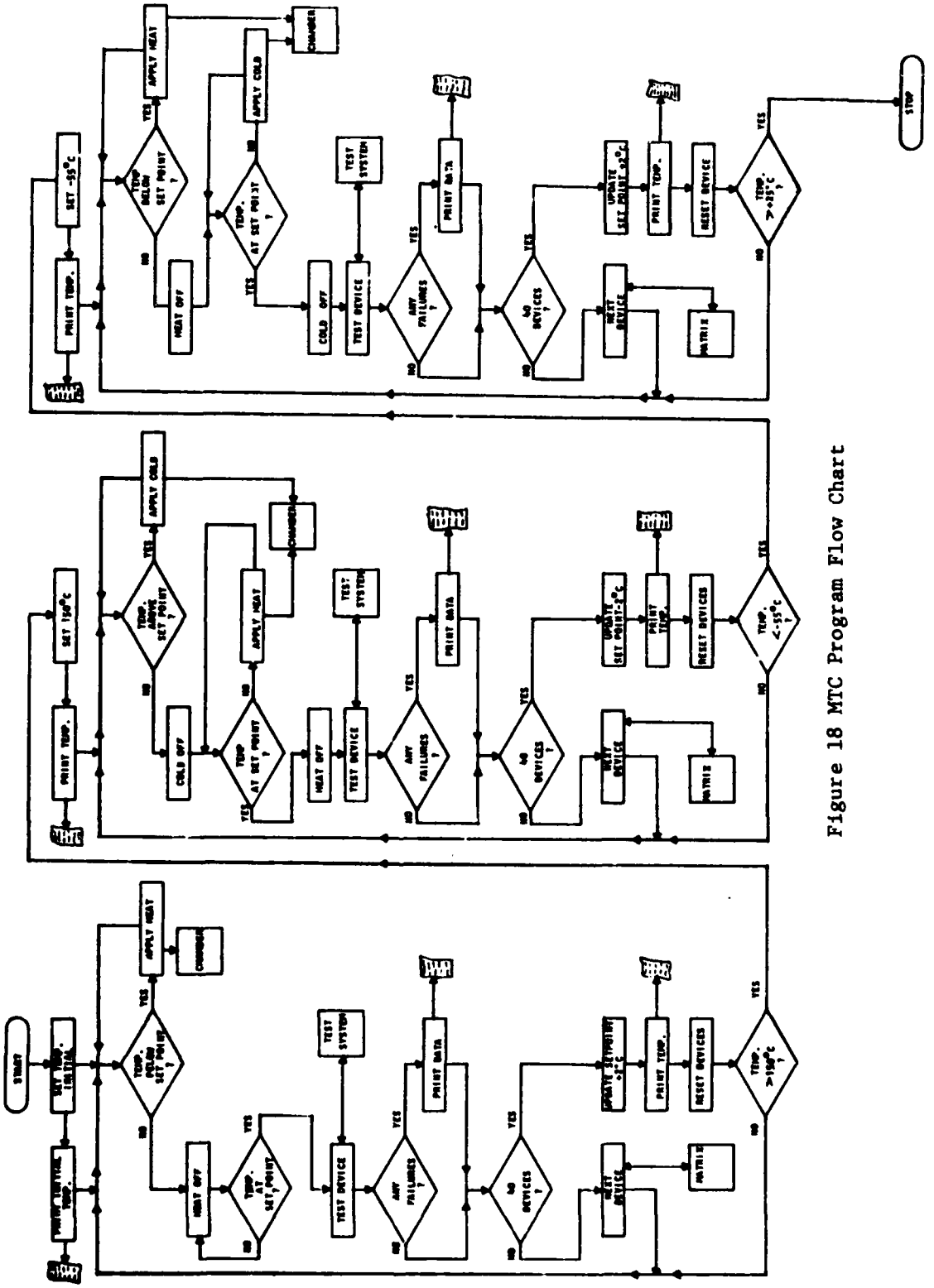


Figure 18 MTC Program Flow Chart

The selection of the device card, and then the socket on the card, was performed with an 8 X 5 matrix of 6 pole reed relays. The pin to be tested was selected by the Teradyne J259 crosspoint matrix. Care was taken to make certain that all relay contacts had settled before the test was started.

Since 40 devices at a time could be tested, it was necessary to make five runs to test the 200 devices in the stress cell. The card locations were made the same for each run so that any potential problems with socket-to-card or card-to-connector connections could be identified through the iterative failure pattern that would be observed.

In addition to the special MTC test, there were two other tests which were not conducted in the conventional manner. The first of these was the steam pressure test. This is usually performed using a pressure cooker which is subject to the evaporation of the water on extended testing. This also allows condensation of the water vapor on the devices during the test. For this program, a chamber was used which resembles an autoclave. The devices were placed in the chamber which can be pre-heated to prevent condensation. The steam is generated outside the chamber and is then admitted into the chamber by a metering valve. This technique permitted continuous operation over long time spans and assured that only dry steam was used. The temperature controller was set so that a few degrees of superheat was used. The use of this chamber also permitted the test to be run at the requested 22.5 psig, which was not attainable in the normal pressure cooker.

The second special test consisted of a measurement to determine if any channeling occurred on the devices that was annealed out rapidly after they were removed from stress. During the high temperature with reverse bias stressing, the devices were allowed to cool to room temperature with the bias still applied. Five of the units were then removed and tested electrically within a few minutes of removal from bias. The balance of that type of device were then read. This process was repeated for each of the device types on stress. After all of the readings had been taken, the first five devices of each type were retested. The first and second readings were then compared for any shift in the electrical parameters indicating the presence of a channel, or inversion layer. There was no significant shift in the first and second readings of the electrical parameters indicating that there was no measureable channel or inversion layer formation and recovery.

SECTION IV

RESULTS OF STRESS TESTS

Significant differences in the number of failures and electrical parameter responses were noted between the plastic and ceramic packaged circuits depending upon the stress. The following discussion highlights the failure and electrical measurement contrasts obtained for the different product types for each stress. For a discussion of the failure modes and mechanisms refer to Section V on failure analysis studies.

Illustrated in Figures 19 and 20 is an overall view of the failure summary contrasts among the vehicle types for each stress identified by the letter code. A qualitative summary ranking of the vehicle types from most to least severe in response to stress is shown in Figure 19. Shown in Figure 20 are the quantitative cumulative failure summary contrasts for the ceramic and plastic packaged vehicles for each stress. Thus,for example, it can be seen that Cell 1 (Temperature Step-Stress with Bias) failures are predominantly Device Type E; Cell 2 (Salt Atmosphere) failures are predominant in Device Type D; relatively few failures for all device types were obtained for Cell 3 (Humidity - Temperature Cycling with Bias); results from Cells 4 and 5 (Humidity Life with Bias) showed a preponderance of failures for Device Types C and E; Cell 6 (Thermal Shock) failures were primarily in Device Type B.

The stress results are summarized in more detail in Figures 21 to 41 for each device type for all six stress cells. Contained in Figures 21 through 28 are the cumulative catastrophic

circuit and TEG failures at each scheduled readout for all the stress cells, contrasting the ceramic and plastic packaged vehicles. The circuit failures are due to gross electrical parameter change. These were manifested in a full scale input offset voltage V_{IO} reading (±16.65 mv) and a very small power supply current ($I_{PS} < 0.1$ ma). The TEG failures shown in Figures 22 and 25 are due to gross transistor element degradation such as catastrophic open or short indications or excessive leakage and/or very low d. c. current gain. Outlined in Figures 29 through 40 are the input offset voltage and power supply current circuit parameter distributions before and after stress. These tables contrast the MIN, MAX, decile and quartile and median percentiles before and after each stress for each of the device type vehicles. Shown in Figure 41 are the input bias current percentiles before and after humidity life with bias stress in the two ceramic types, A and B and plastic type D.

The temperature step-stress with applied reverse bias, Cell 1, shows an excessive number of failures for device type E. Reference to Figure 21 shows 30% of these failures occurring after the first 100°C step. These failures exhibited full scale V_{IO} readings (±16.65 mv) and indicated a zero I_{IB} reading. The I_{PS} readings were not affected. This can be seen by referring to Figures 29 and 30.

Contained in Figure 22 are the TEG cumulative failures on temperature with bias stressing. These also show excessive failures for device type, ET and correlate well with the circuit failures. The TEGs stressed here correspond to device

types A, C, and E are identified as AT, CT and ET, respectively.

The 72 hour salt atmosphere exposure, Cell 2, shows excessive failures for plastic silicone device Type, D. Most of these failures occurred after 48 hours of stress. This is noted in Figure 23. The failures occurring here showed full scale V_{IO} measurements with some effect on I_{PS} values. This can be seen by referring to Figures 31 and 32 where the percentiles of V_{IO} and I_{PS} are given befcre after salt spray exposure.

After 1000 hours of humidity and temperature cycling from 25°C to 65°C, with bias, Cell 3, three of the device types (A, C, D) showed zero failures while the other two were 10% and under. The relatively few failures obtained here exhibited not only full scale V_{IO} values but also very small I_{PS} readings, thereby appearing as opens. Contained in Figures 24, 33 and 34 are the failure and electrical parameter response-to-stress summaries by device types. In Figure 25 are the TEG cumulative failure summaries, which show excessive transistor parameter element failures for the ET type.

The steady state humidity life of 85°C, 85% RH with bias proved to be most severe for device types C and E. The failures appeared as catastrophic opens with full scale voltage reading for V_{IO} and insignificant I_{PS} values, i.e. from pre-stress milliampere readings to post-stress nanoamperes values. The failure summaries and electrical parameter response are shown in Figures 26, 27, 35, 36, 37 and 38 respectively. The input bias current (I_{IB}) response to humidity life with bias is shown in Figure 41 for device types A, B and D. For device types C and E, where failures were excessive after this stress, the I_{IB} readings were zero.

Temperature-time profiles of a sample of circuits that failed monitored temperature cycling are shown in Figures 42 through 48. As shown in the profile, a complete cycle starts at 25°C, increases to 151°C, decreases to -55°C and returns to 25°C. This is done in two degree increments, with a slope of approximately 2°C/minute. Identity of the card, device number and pin number is made when a unit under test fails by indicating an open circuit. There was poor unit-to-unit correlation between the monitored temperature cycling failure indicators and those that failed the subsequent stress-in-time of humidity life with bias, Cell 5.

Shown in Figures 42 through 47 are the temperature-time profiles of the three units failing both the first and second cycle of the monitored temperature cycling. These failures are noted in the failure summary of Cell 5 in Figure 27. Both the first and second cycle traces are given and it can be seen that the failure indication region is predominantly in the higher temperature portion of the cycle. In all cases the second cycle repeats and extends the failure indication region. Shown in Figure 48 is a temperature-time profile of a device indicating failure on the second monitored cycle only.

Poor unit-to-unit correlation was obtained between monitored temperature cycle failure indicators and failures on humidity life with bias. The test results showed that, among the units indicating monitored temperature cycle failure, there were approximately equal numbers failing and not failing the subsequent humidity life with bias stress. The same was also true about

the units that were non-failure indicators on monitored temperature cycle.

The short term preconditioning of steam pressure and bake, Cell 4, did not appear to have a significant effect on the subsequent long term humidity life with bias performance for Device Types A, B, C and E. This can be seen by comparing the humidity and bias failure results of Figure 25 with Figure 26, where the results shown in the latter figure are for those devices not having steam pressure and bake preconditioning. The failure results by device are not significantly different for Device Types A, B, C and E. There is a difference for Device Type D which shows a significantly greater failure percentage for those units having the steam pressure preconditioning.

The 50 cycles of air-to-air temperature cycling, Cell 6, produced no failures for all packaged device types. The subsequent liquid-to-liquid thermal shock stressing revealed excessive failures for the ceramic type B. The nature of these failures are described in the failure analysis section. The failure summaries and electrical parameter responses are shown by device type in Figures 28, 39 and 40.

RANKED SUMMARY OF STRESSES AND PACKAGE TYPE

STRESS	DEVICE RESPONSE (RANKED FROM MAXIMUM TO MINIMUM RESPONSE) GREATER THAN 10% FAILURE	UNDER AND INCLUDING 10% FAILURE	FAILURE FREE
TEMPERATURE WITH BIAS	E	C,B,D,A	
SALT ATMOSPHERE	D	A	B,C,E
HUMIDITY TEMPERATURE WITH BIAS		E,B	A,C,D
HUMIDITY LIFE WITH BIAS	C,E,B	D,A,	
TEMPERATURE CYCLING	ALL FAILURE FREE		
THERMAL SHOCK	B,C	E,A	D

Figure 19 Ranked Summary Response To Stress of Device Types

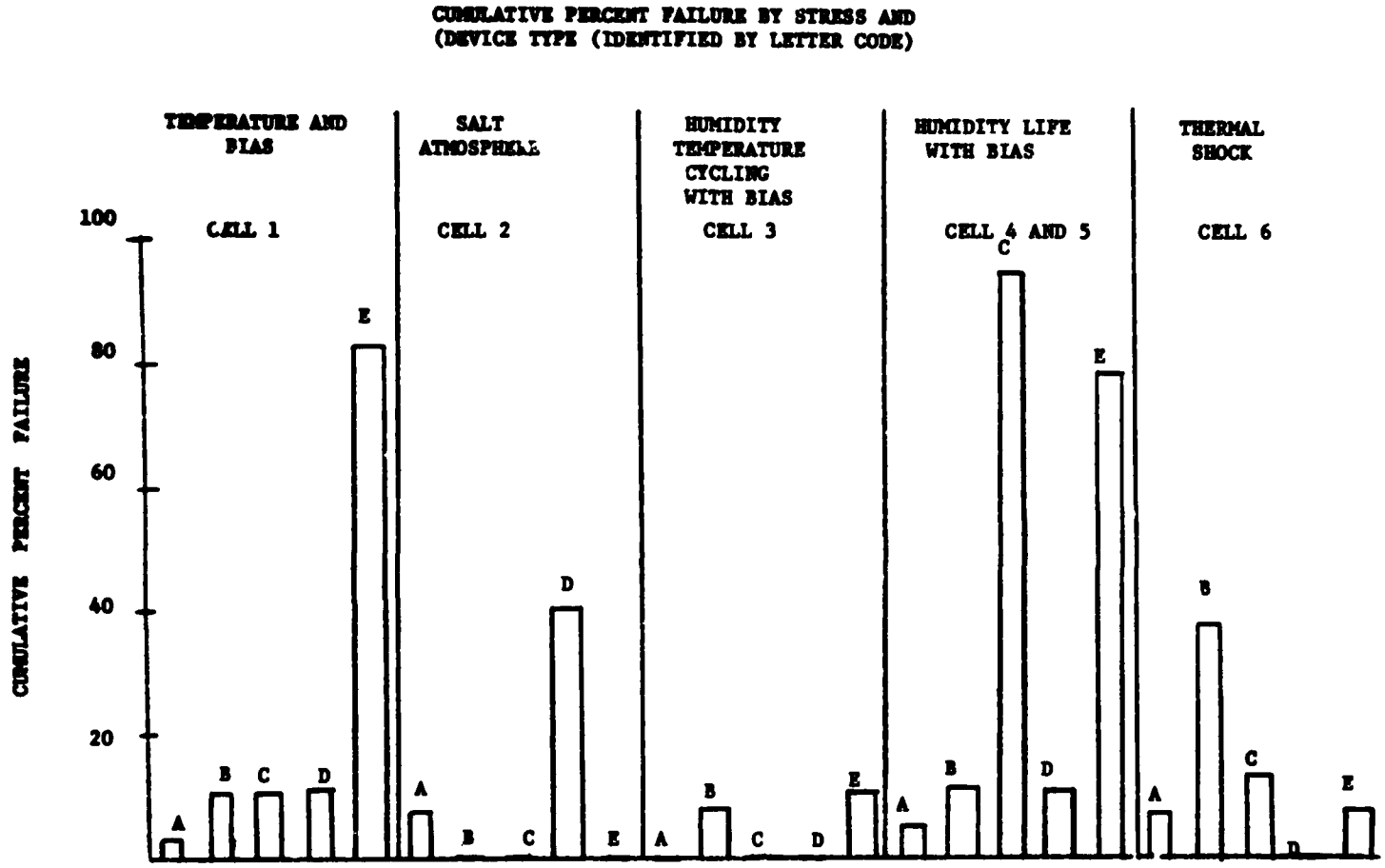


Figure 20 Cumulative Percent Failure of Device Type By Stress

CUMULATIVE FAILURES* CELL 1

TEMPERATURE STEP-STRESS IN °C

N = 30 SAMPLES PER TYPE

Device Type	100	125	150	175	200
A	0	0	1	1	1 (3%)
B	0	0	2	3	3 (10%)
C	1	1	3	3	3 (10%)
D	0	0	0	3	3 (10%)
E	9	17	19	24	25 (83%)

*Catastrophic Failure Indication - Opens or Shorts

Figure 21 Cumulative Failures of Device Types for Cell 1

CUMULATIVE TEG FAILURES* CELL 1

TEMPERATURE STEP-STRESS WITH BIAS

DEVICE TYPE	SAMPLE SIZE	TEMPERATURE STEP IN °C			
		100	150	175	200
AT	26	0 (0%)	0 (0%)	1 (4%)	1 (4%)
CT	73	22 (30%)	30 (41%)	31 (42%)	31 (42%)
ET	36	10 (28%)	31 (86%)	32 (89%)	33 (92%)

*Catastrophic Failure Indication - Opens or Shorts

Degradation Failure I_{CBO} or I_{EBO} >1μA

Figure 22 Cumulative TEG Failures of Device Types for Cell 1

CUMULATIVE FAILURES* CELL 2

SALT ATMOSPHERE

N = 30 SAMPLES PER TYPE

DEVICE TYPE	STRESS TIME IN HOURS 24	48	72
A	0	0	2 (7%)
B	0	0	0 (0%)
C	0	0	0 (0%)
D	1	9	12 (40%)
E	0	0	0 (0%)

*Catastrophic Failure Indication - Opens or Shorts

Figure 23 Cumulative Failures of Device Types for Cell 2

CUMULATIVE FAILURES* CELL 3

HUMIDITY-TEMPERATURE CYCLING WITH BIAS

N = 40 SAMPLES PER TYPE

DEVICE TYPE	STRESS 16ℰ	TIME IN HOURS 500	1000
A	0	0	0 (0%)
B	1	1	3 (8%)
C	0	0	0 (0%)
D	0	0	0 (0%)
F	1	2	4 (10%)

*Catastrophic Failure Indication - Opens or Shorts

Figure 24 Cumulative Failures of Device Types for Cell 3

CUMULATIVE TEG FAILURES* CELL 3

HUMIDITY-TEMPERATURE CYCLING WITH BIAS

DEVICE TYPE	SAMPLE SIZE	STRESS TIME IN HOURS	
		168	1000
AT	78	2 (3%)	22 (28%)
CT	78	2 (3%)	22 (28%)
ET	39	19 (49%)	39 (100%)

* Catastrophic Failure Indication - Opens or Shorts
Degradation Failure I_{CBO} or I_{EBO} > 1μA

Figure 25 Cumulative TEG Failures of Device Types for Cell 3

CUMULATIVE FAILURES* CELL 4

STEAM PRESSURE/HUMIDITY LIFE WITH BIAS

N = 40 SAMPLES PER TYPE

DEVICE TYPE	STRESS TIME IN HOURS									
	STEAM PRESSURE					HUMIDITY LIFE WITH BIAS				
	4	8	12	24	48	168	500	1000	3000	
A	0	0	0	0	0	0	0	2	2	(5%)
B	0	0	0	0	0	0	1	3	4	(10%)
C	1	1	1	1	1	1	20	39	39	(98%)
D	0	0	0	0	0	0	0	3	7	(18%)
E	0	0	0	0	0	1	6	21	32	(80%)

*CATASTROPHIC FAILURE INDICATION - OPENS OR SHORTS

Figure 26 Cumulative Failures of Device Types for Cell 4

CUMULATIVE FAILURES* CELL 5

TEMPERATURE CYCLING/HUMIDITY LIFE WITH BIAS

(2 CYCLES MONITORED)

N = 40 SAMPLES PER TYPE

DEVICE TYPE	CYCLES OF STRESS TEMPERATURE CYCLING: FAILURE INDICATORS AFTER 1ST MONITORED CYCLE	CYCLES OF STRESS TEMPERATURE CYCLING: AFTER 20 CYCLES OF TEMPERATURE CYCLING (UN-MONITORED)	CYCLES OF STRESS TEMPERATURE CYCLING: FAILURE INDICATORS AFTER 2ND MONITORED CYCLE	STRESS TIME IN HOURS HUMIDITY LIFE WITH BIAS: 168	500	1000	2000
A	0	0	2	1	1	1	2 (5%)
B	2***	0	2***	0	3	4	5 (12%)
C	0	0	7	0	21	35	36 (90%)
D	1**	1**	1**	1	1	1	1 (2%)
E	0	0	3	2	6	18	30 (75%)

* CATASTROPHIC FAILURE INDICATIONS - OPENS or SHORTS

** SAME UNIT - READS AS INTERMITTENT/DID NOT FAIL HUMIDITY LIFE

***SAME UNITS - READ AS INTERMITTENTS/ONE UNIT FAILED HUMIDITY LIFE INITIALLY

Figure 27 Cumulative Failures of Device Types for Cell 5

CUMULATIVE FAILURES CELL 6

TEMPERATURE CYCLING/THERMAL SHOCK

N = 30 SAMPLES PER TYPE

DEVICE TYPE	CYCLES OF STRESS						
	TEMPERATURE CYCLING			THERMAL SHOCK			
	10	20	50	10	20	50	
A	0	0	0	2	2	2	(7%)
B	0	0	0	0	0	11	(37%)
C	0	0	0	0	0	4	(13%)
D	0	0	0	0	0	0	(0%)
E	0	0	0	0	1	2	(7%)

* CATASTROPHIC FAILURE INDICATION - OPENS or SHORTS

Figure 28 Cumulative Failures of Device Types for Cell 6

INPUT OFFSET VOLTAGE (V_{IO}) RESPONSE TO TEMPERATURE
STEP-STRESS WITH BIAS (CELL 1)

30 SAMPLES PER DEVICE TYPE

V_{IO} in mV

DEVICE TYPE	PERCENTILES	INITIAL	AFTER 125°C	AFTER 150°C	AFTER 200°C
A	MIN	-3.61	-3.67	-3.54	-3.79
	10	-2.80	-2.89	-2.61	-2.73
	25	-2.16	-2.28	-2.27	-2.22
	50	-0.81	-0.86	-0.96	-0.98
	75	-0.34	-0.37	0.24	0.21
	90	0.75	0.74	1.96	3.52
	MAX	3.88	3.82	16.65	16.65
B	MIN	-4.04	-3.99	-16.65	-16.65
	10	-1.67	-1.69	-3.75	-3.75
	25	-0.60	-0.60	-0.99	-0.88
	50	-0.02	0.07	0.00	-0.04
	75	0.54	0.58	0.61	0.76
	90	1.85	1.75	1.63	1.63
	MAX	2.80	2.78	2.81	2.78
C	MIN	-3.49	-3.82	-16.65	-16.65
	10	-2.85	-3.16	-3.34	-3.25
	25	-1.24	-1.47	-1.88	-1.65
	50	-0.28	-0.14	-0.58	-0.06
	75	0.62	1.06	1.73	1.65
	90	2.15	1.95	4.61	2.43
	MAX	2.35	16.65	16.65	16.65
D	MIN	-2.06	-2.08	-5.25	-3.25
	10	-1.72	-1.71	-1.62	-1.31
	25	-0.76	-0.70	-0.78	-0.40
	50	-0.21	-0.03	0.27	-0.05
	75	1.03	1.08	1.33	0.96
	90	1.78	1.63	3.69	3.08
	MAX	3.46	3.54	4.82	16.65
E	MIN	-3.92	-16.65	-16.65	-16.65
	10	-1.48	-13.84	-16.65	-16.65
	25	-0.84	-0.56	-16.65	-16.65
	50	-0.18	1.35	-9.10	-16.65
	75	0.80	16.65	0.87	-0.52
	90	1.24	16.65	9.93	16.65
	MAX	2.68	16.65	16.65	16.65

Figure 29 Input Offset Voltage Response of Cell 1

POWER SUPPLY CURRENT DRAIN (I_{PS}) RESPONSE TO TEMPERATURE STEP-STRESS WITH BIAS. (CELL 1)

30 SAMPLES PER DEVICE TYPE

I_{PS} in mA (UNLESS OTHERWISE NOTED)

DEVICE TYPE	PERCENTILES	INITIAL	AFTER 125°C	AFTER 150°C	AFTER 200°C
A	MIN	0.99	1.00	55 uA	55 uA
	10	1.04	1.05	1.01	1.03
	50	1.57	1.58	1.50	1.47
	75	1.82	1.75	1.74	1.72
	90	2.01	2.02	2.02	2.01
	MAX	2.07	2.07	2.02	2.05
B	MIN	1.06	1.03	1.03	1.03
	10	1.17	1.18	1.21	1.17
	25	1.28	1.29	1.28	1.28
	50	1.65	1.53	1.66	1.77
	75	2.04	1.99	2.02	2.02
	90	2.11	2.30	2.26	2.32
	MAX	2.58	2.61	2.61	2.60
C	MIN	0.58	0.58	28 nA	28 nA
	10	0.96	0.97	0.96	0.94
	25	1.13	1.14	1.11	1.11
	50	1.49	1.49	1.39	1.32
	75	1.66	1.66	1.75	1.61
	90	1.98	2.05	1.89	1.91
	MAX	2.16	2.47	2.20	2.15
D	MIN	0.83	0.83	0.84	0.86
	10	0.87	0.88	0.89	0.92
	25	0.96	0.96	0.92	0.95
	50	1.58	1.59	1.46	1.64
	75	1.70	1.78	1.77	1.85
	90	1.94	1.92	1.92	2.03
	MAX	2.10	2.11	2.13	2.22
E	MIN	0.90	0.80	0.89	0.92
	10	0.97	0.95	1.08	1.21
	25	1.08	1.16	1.49	1.50
	50	1.41	1.34	1.81	1.79
	75	1.73	1.61	1.92	2.04
	90	1.84	1.82	2.16	2.17
	MAX	1.96	1.91	2.69	2.69

Figure 30 Power Supply Current Drain Response of Cell 1

INPUT OFFSET VOLTAGE (V_{IO}) RESPONSE TO SALT ATMOSPHERE

(CELL 2)

40 SAMPLES PER DEVICE TYPE

V_{IO} In mV

DEVICE TYPE	PERCENTILES	INITIAL	AFTER 72 HOURS
A	MIN	-3.38	-16.65
	10	-2.42	- 3.37
	25	-1.38	- 1.37
	50	0.13	0.00
	75	0.98	1.11
	90	2.20	2.56
	MAX	3.26	16.65
B	MIN	-3.12	- 3.11
	10	-1.88	- 1.87
	25	-0.67	- 0.66
	50	-0.07	- 0.03
	75	0.55	0.56
	90	1.39	1.40
	MAX	3.09	3.09
C	MIN	-4.40	- 4.29
	10	-2.56	- 1.48
	25	-0.96	0.77
	50	0.64	0.89
	75	2.11	2.25
	90	2.91	3.32
	MAX	3.37	4.92
D	MIN	-3.07	-16.65
	10	-2.14	-15.18
	25	-1.04	- 0.85
	50	-0.56	0.34
	75	0.63	16.65
	90	1.84	16.65
	MAX	2.76	16.65
E	MIN	-4.26	- 4.18
	10	-3.13	- 2.11
	25	-1.50	- 1.40
	50	-0.36	- 0.32
	75	0.86	0.94
	90	2.18	2.22
	MAX	2.76	2.78

Figure 31 Input Offset Voltage Response of Cell 2

POWER SUPPLY CURRENT DRAIN (I_{PS}) RESPONSE TO SALT ATMOSPHERE

(CELL 2), 30 SAMPLES PER DEVICE TYPE

I_{PS} in mA UNLESS OTHERWISE NOTED

DEVICE TYPE	PERCENTILES	INITIAL	AFTER 72 HOURS
A	MIN	0.96	38 nA
	10	1.06	0.96
	25	1.15	1.14
	50	1.38	1.37
	75	1.68	1.72
	90	1.91	2.02
	MAX	2.07	6.78
B	MIN	1.04	1.04
	10	1.07	1.07
	25	1.32	1.32
	50	1.62	1.62
	75	1.75	1.91
	90	2.08	2.08
	MAX	2.49	2.49
C	MIN	0.85	0.85
	10	1.02	1.01
	25	1.09	1.08
	50	1.32	1.32
	75	1.51	1.54
	90	1.79	1.81
	MAX	2.05	2.05
D	MIN	0.78	17 nA
	10	0.85	54 uA
	25	0.95	0.89
	50	1.58	1.03
	75	1.74	1.71
	90	1.91	1.91
	MAX	1.94	3.68
E	MIN	0.96	0.96
	10	1.08	1.08
	25	1.18	1.18
	50	1.45	1.41
	75	1.72	1.72
	90	1.85	1.85
	MAX	2.13	2.14

Figure 32 Power Supply Current Drain Response of Cell 2

INPUT OFFSET VOLTAGE (V_{IO}) RESPONSE TO HUMIDITY-TEMPERATURE CYCLING WITH BIAS (CELL 3)

40 SAMPLES PER Device Type

V_{IO} in mV

DEVICE TYPE	PERCENTILES	INITIAL	AFTER 1000 HRS.
A	MIN.	-4.32	-4.18
	10	-3.90	-3.30
	25	-1.82	-2.34
	50	-0.83	-0.82
	75	0.30	0.33
	90	2.14	2.21
	MAX	3.71	3.61
B	MIN	-4.07	-12.48
	10	-2.48	-2.58
	25	-1.48	-1.35
	50	-0.59	-0.55
	75	0.49	0.54
	90	2.48	3.39
	MAX	4.04	16.65
C	MIN	-2.74	-2.37
	10	-1.85	-1.49
	25	-1.07	-0.78
	50	0.13	0.42
	75	1.39	1.57
	90	2.22	2.30
	MAX	4.06	4.82
D	MIN	-2.69	-2.62
	10	-2.09	-1.98
	25	-1.32	-1.22
	50	0.42	0.45
	75	1.12	1.11
	90	1.49	1.61
	MAX	2.72	2.65
E	MIN	-3.84	-16.65
	10	-1.65	-3.86
	25	-1.05	-1.01
	50	0.06	-0.04
	75	1.46	1.85
	90	2.76	2.88
	MAX	3.07	16.65

Figure 33 Input Offset Voltage Response of Cell 1

POWER SUPPLY CURRENT DRAIN (I_{PS}) RESPONSE TO HUMIDITY-TEMPERATURE CYCLING WITH BIAS (CELL 3)

40 SAMPLES PER DEVICE TYPE

I_{PS} In mA UNLESS OTHERWISE NOTED

DEVICE TYPE	PERCENTILES	INITIAL	AFTER 1000 HRS.
A	MIN	0.85	0.85
	10	1.07	1.08
	25	1.19	1.20
	50	1.52	1.56
	75	1.75	1.78
	90	1.97	2.01
	MAX	2.03	2.05
B	MIN	0.97	0.99
	10	1.20	1.19
	25	1.35	1.30
	50	1.73	1.68
	75	1.98	2.08
	90	2.28	2.35
	MAX	2.61	3.21
C	MIN	0.78	0.77
	10	0.94	0.95
	25	1.07	1.05
	50	1.35	1.28
	75	1.52	1.53
	90	1.87	1.88
	MAX	1.92	1.92
D	MIN	0.72	0.73
	10	0.84	0.85
	25	0.88	0.87
	50	1.07	1.02
	75	1.70	1.72
	90	1.82	1.88
	MAX	2.08	2.05
E	MIN	0.83	62 nA
	10	0.98	0.86
	25	1.17	1.17
	50	1.33	1.43
	75	1.82	1.91
	90	1.93	3.92
	MAX	2.16	7.44

Figure 34 Power Supply Current Drain Response of Cell 3

INPUT OFFSET VOLTAGE (V_{IO}) RESPONSE TO STEAM PRESSURE/ HUMIDITY AND BIAS (CELL 4)

40 SAMPLES PER DEVICE TYPE

V_{IO} In mV

DEVICE TYPE	PERCENTILES	INITIAL	48 HOURS PRESSURE COOKER	HUMIDITY LIFE & BIAS 1000 HOURS	3000 HOURS
A	MIN.	-4.16	-4.18	-4.16	-4.15
	10	-2.44	-2.48	-2.54	-2.40
	25	-0.93	-1.00	-0.95	-0.82
	50	-0.40	-0.17	-0.26	-0.12
	75	0.48	0.40	0.58	0.67
	90	1.71	1.69	2.11	2.06
	MAX	2.72	2.68	16.65	16.65
B	MIN.	-2.57	-2.61	-2.62	-16.65
	10	-1.97	-2.03	-1.73	-2.09
	25	-1.17	-1.03	-1.1	-1.26
	50	-0.2	-0.24	-0.18	-0.22
	75	0.71	0.68	1.20	1.58
	90	1.65	1.64	3.01	15.29
	MAX	3.03	3.07	16.65	16.65
C	MIN.	-3.69	-3.18	-16.65 mV	-16.65
	10	-2.32	-2.13	-16.65	-16.65
	25	-1.58	-1.54	-16.65	-16.65
	50	-0.40	-0.04	-16.65	-16.65
	75	0.59	0.88	-16.65	-16.65
	90	2.22	2.19	0.39	0.33
	MAX	4.16	3.79	16.65	16.65
D	MIN.	-2.32	-2.08	-16.65	-16.65
	10	-1.48	-1.21	-1.96	-16.12
	25	-0.76	-0.50	-0.42	-0.12
	50	0.45	0.66	0.45	0.95
	75	1.52	1.67	1.71	2.12
	90	2.07	2.27	2.94	3.60
	MAX	3.28	3.36	16.65	16.65
E	MIN.	-3.91	-3.69	-16.65	-16.65
	10	-2.91	-2.66	-16.65	-16.65
	25	-1.32	-1.22	-1.28	-16.65
	50	-0.62	-0.31	0.40	0.32
	75	0.58	0.67	16.65	16.65
	90	2.06	2.04	16.65	16.65
	MAX	3.15	3.28	16.65	16.65

Figure 35 Input Offset Voltage Response of Cell 4

POWER SUPPLY CURRENT DRAIN (I_{PS}) RESPONSE TO STEAM PRESSURE/ HUMIDITY AND BIAS (CELL 4)

40 SAMPLES PER DEVICE TYPE

I_{PS} In mA UNLESS OTHERWISE NOTED

DEVICE TYPE	PERCENTILES	INITIAL	48 HOURS PRESSURE COOKER	HUMIDITY LIFE & BIAS 1000 HOURS	3000 HOURS
	MIN	0.95	0.95	0.96	0.96
	10	1.03	1.04	1.04	1.02
A	25	1.29	1.28	1.16	1.14
	50	1.49	1.49	1.48	1.49
	75	1.68	1.68	1.71	1.70
	90	1.91	1.91	1.92	1.92
	MAX	2.02	2.05	2.06	2.07
	MIN	1.05	1.05	1.06	1.06
	10	1.22	1.22	1.19	1.22
B	25	1.31	1.34	1.31	1.31
	50	1.75	1.75	1.68	1.80
	75	1.88	1.91	2.08	2.11
	90	2.25	2.27	2.32	2.34
	MAX	2.40	2.45	2.45	2.95
	MIN	0.79	0.77	0 nA	0 nA
	10	1.09	1.09	7 nA	7 nA
C	25	1.23	1.16	19 nA	19 nA
	50	1.50	1.38	26 nA	26 nA
	75	1.72	1.72	29 nA	29 nA
	90	1.93	1.94	1.23	3.01
	MAX	2.03	2.03	4.15	8.05
	MIN	0.76	0.82	21 nA	21 nA
	10	0.84	0.91	0.92	0.86
D	25	0.91	0.96	0.98	1.00
	50	1.05	1.10	1.09	1.06
	75	1.57	1.83	1.74	1.60
	90	1.76	1.91	1.92	1.96
	MAX	1.86	2.03	2.07	2.03
	MIN	0.79	0.80	33 nA	10 nA
	10	1.01	1.01	59 nA	22 nA
E	25	1.24	1.24	1.01	60 nA
	50	1.60	1.57	1.75	0.73
	75	1.81	1.81	3.94	2.58
	90	2.03	2.03	6.55	4.94
	MAX	2.27	2.28	8.82	8.82

Figure 36 Power Supply Current Drain Response of Cell 4

INPUT OFFSET VOLTAGE (V_{IO}) RESPONSE TO TEMPERATURE CYCLING/
HUMIDITY AND BIAS (CELL 5)

40 SAMPLES PER DEVICE TYPE

V_{IO} In mV

DEVICE TYPE	PERCENTILES	INITIAL	22 CYCLES OF TEMPERATURE CYCLING	HUMIDITY LIFE & BIAS 1000 HRS	2 [illegible] HRS
A	MIN	-4.08	-4.01	-3.98	-16.65
	10	-2.80	-2.70	-2.58	-3.70
	25	-2.12	-1.77	-1.83	-2.04
	50	-0.58	-0.59	-0.58	-0.61
	75	0.70	0.7[illegible]	0.84	0.80
	90	1.09	1.1[illegible]	1.91	1.86
	MAX	2.11	2.12	16.65	16.65
B	MIN	-3.62	-3.66	-16.65	-16.65
	10	-2.05	-2.04	-9.05	-[illegible].08
	25	-1.14	-1.07	-1.33	-2.02
	50	0.14	0.19	-0.24	-0.66
	75	0.82	0.84	0.97	0.97
	90	1.77	2.18	2.[illegible]8	3.11
	MAX	2.36	2.38	16.65	16.65
C	MIN	-[illegible].10	-4.93	-16.65	-16.65
	10	-2.38	.43	-16.65	-16.65
	25	-0.73	-0.70	-16.65	-16.65
	50	-0.22	-0.07	-16.65	-16.65
	75	1.43	1.40	-1.25	-1.25
	90	3.20	3.01	.84	1.84
	MAX	3.87	3.95	16.65	16.65
D	MIN	-2.41	-2.42	-16.65	-16.65
	10	-1.72	-1.70	-2.99	-0.86
	25	-0.68	-0.66	-0.[illegible]0	-0.02
	50	0.32	0.34	0.54	0.59
	[illegible]	1.94	1.94	1.60	2.0[illegible]
	[illegible]	3.34	3.40	3.45	3.45
	MA[illegible]	4.20	4.1[illegible]	4.31	4.76
[illegible]	MIN	-2.86	-3.06	-16.65	-16.65
	10	-2.79	-2.7[illegible]	-3.10	-16.65
	[illegible]	-1.19	-1.03	0.33	0.32
	50	0.18	0.05	1.66	16.65
	[illegible]	1.02	0.97	14.77	16.65
	9[illegible]	1.90	2.08	16.65	16.65
	MAX	2.8[illegible]	2.82	16.[illegible]5	16.65

Figure 37 Input Offset voltage Response of Cell 5

POWER SUPPLY CURRENT DRAIN (I_{PS}) RESPONSE TO TEMPERATURE CYCLING/HUMIDITY AND BIAS. CELL 5

40 SAMPLES PER DEVICE TYPE

I_{PS} in mA UNLESS OTHERWISE NOTED

DEVICE TYPE	PERCENTILES	INITIAL	22 CYCLES OF TEMPERATURE CYCLING	HUMIDITY LIFE & BIAS 1000 HRS.	2000 HRS
	MIN	0.94	0.94	0.94	0.94
	10	1.10	1.13	1.13	1.14
A	25	1.29	1.26	1.31	1.24
	50	1.40	1.39	1.41	1.39
	75	1.65	1.56	1.68	1.56
	90	1.88	1.82	1.87	1.82
	MAX	1.92	1.92	1.95	1.94
	MIN	0.95	0.96	0.95	1.01
	10	1.08	1.08	1.22	1.28
B	25	1.32	1.30	1.32	1.35
	50	1.56	1.49	1.72	1.62
	75	1.81	1.81	1.97	1.96
	90	2.04	2.03	2.13	2.10
	MAX	2.29	2.26	2.45	2.52
	MIN	0.88	0.87	14 nA	14 nA
	10	0.99	0.98	20 nA	22 nA
C	25	1.18	1.14	26 nA	26 nA
	50	1.42	1.39	52 nA	52 nA
	75	1.56	1.57	806 uA	806 uA
	90	1.73	1.74	1.61	1.61
	MAX	1.92	1.92	1.72	4.35
	MIN	0.82	0.82	0.82	0.85
	10	0.84	0.84	0.87	0.87
D	25	0.91	0.91	0.92	0.94
	50	1.02	1.02	1.08	1.03
	75	1.68	1.64	1.71	1.76
	90	1.86	1.82	1.86	1.92
	MAX	1.92	1.87	1.92	1.97
	MIN	0.92	0.93	22 nA	22 nA
	10	1.03	1.04	58.9 uA	59.0uA
E	25	1.15	1.14	1.09	1.13
	50	1.42	1.39	1.50	2.1
	75	1.71	1.71	2.55	4.78
	90	1.87	1.88	5.32	7.36
	MAX	2.19	2.20	6.74	10.76

Figure 38 Power Supply Current Drain Response of Cell 5

INPUT OFFSET VOLTAGE (V_{IO}) RESPONSE TO THERMAL SHOCK

(CELL 6)

30 SAMPLES PER DEVICE TYPE

V_{IO} in mV

DEVICE TYPE	PERCENTILES	INITIAL	AFTER 50 CYCLES
A	MIN	-4.49	-4.34
	10	-3.26	-3.16
	25	-1.41	-1.12
	50	-0.46	-0.44
	75	0.27	0.62
	90	1.50	1.48
	MAX	2.48	2.46
B	MIN	-3.66	-16.65
	10	-2.32	-2.50
	25	-1.27	-0.64
	50	-0.42	-0.07
	75	1.45	1.31
	90	2.49	3.64
	MAX	3.92	16.65
C	MIN	-3.27	-16.65
	10	-2.90	-15.29
	25	-1.50	-1.74
	50	0.13	0.10
	75	1.40	1.61
	90	2.34	2.73
	MAX	3.84	4.04
D	MIN	-3.28	-3.22
	10	-1.51	-1.64
	25	-0.76	-0.93
	50	-0.32	0.23
	75	1.36	1.47
	90	1.91	2.06
	MAX	3.23	3.21
E	MIN	-3.20	-16.65
	10	-1.78	-3.10
	25	-1.08	-1.20
	50	0.32	0.11
	75	1.53	1.54
	90	2.08	1.94
	MAX	2.61	2.38

Figure 39 Input Offset Voltage Response of Cell 6

POWER SUPPLY CURRENT DRAIN (I_{PS}) RESPONSE TO THERMAL SHOCK

(CELL 6)

30 SAMPLES PER DEVICE TYPE

I_{PS} In mA UNLESS OTHERWISE NOTED

DEVICE TYPE	PERCENTILES	INITIAL	AFTER 50 CYCLES
A	MIN	1.06	1.06
	10	1.09	1.09
	25	1.25	1.25
	50	1.46	1.45
	75	1.76	1.76
	90	1.92	1.92
	MAX	1.95	1.96
B	MIN	0.98	55 uA
	10	1.07	1.03
	25	1.22	1.17
	50	1.55	1.60
	75	1.81	1.74
	90	2.03	2.25
	MAX	2.49	7.85
C	MIN	0.51	334 nA
	10	1.02	0.55
	25	1.08	1.06
	50	1.28	1.25
	75	1.62	1.60
	90	1.79	1.80
	MAX	2.05	2.06
D	MIN	0.76	0.77
	10	0.81	0.81
	25	0.88	0.88
	50	1.26	1.54
	75	1.72	1.74
	90	1.78	1.82
	MAX	2.25	2.26
E	MIN	0.73	42 nA
	10	0.97	0.95
	25	1.16	1.19
	50	1.24	1.26
	75	1.58	1.59
	90	1.75	1.76
	MAX	2.18	2.21

Figure 40 Power Supply Current Drain Response of Cell 6

INPUT BIAS CURRENT (I_{IB}) RESPONSE ON HUMIDITY LIFE WITH BIAS

I_{IB} In nA

CELL 4

DEVICE TYPE	PERCENTILES	INITIAL	AFTER 3000 HOURS
A	10	56	56
	50	88	93
	90	135	142
B	10	14	8
	50	32	29
	90	62	56
D	10	29	0*
	50	7[illegible]	115
	90	135	155

CELL 5

DEVICE TYPE	PERCENTILES	INITIAL	AFTER 2000 HOURS
A	10	48	55
	50	80	92
	90	130	140
B	10	15	14
	50	30	26
	90	62	64
D	10	42	100
	50	84	160
	90	143	230

* DUE TO CATASTROPHIC FAILURE

Figure 41 Input Bias Current Response for Cell 5

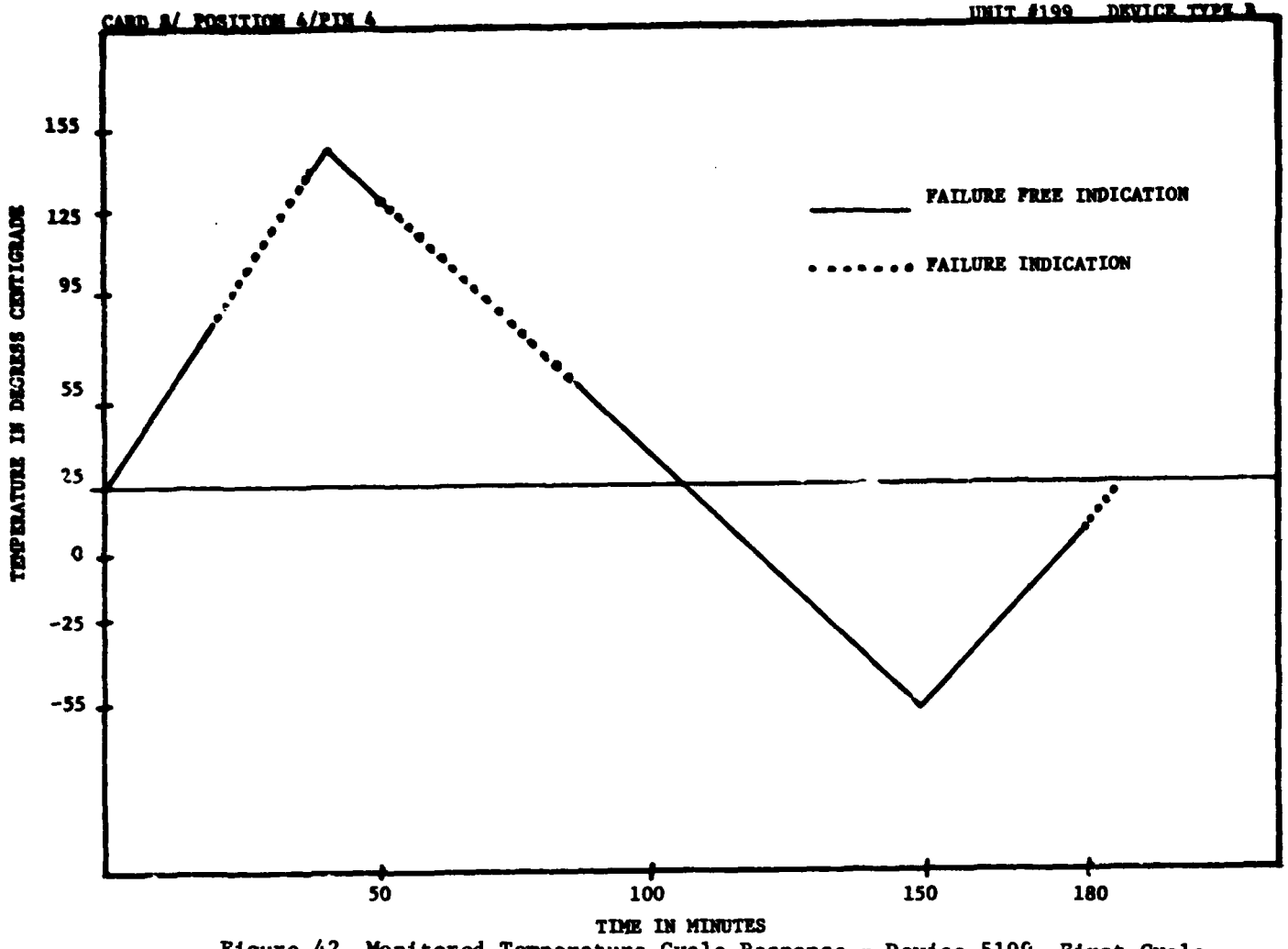


Figure 42 Monitored Temperature Cycle Response - Device 5199, First Cycle

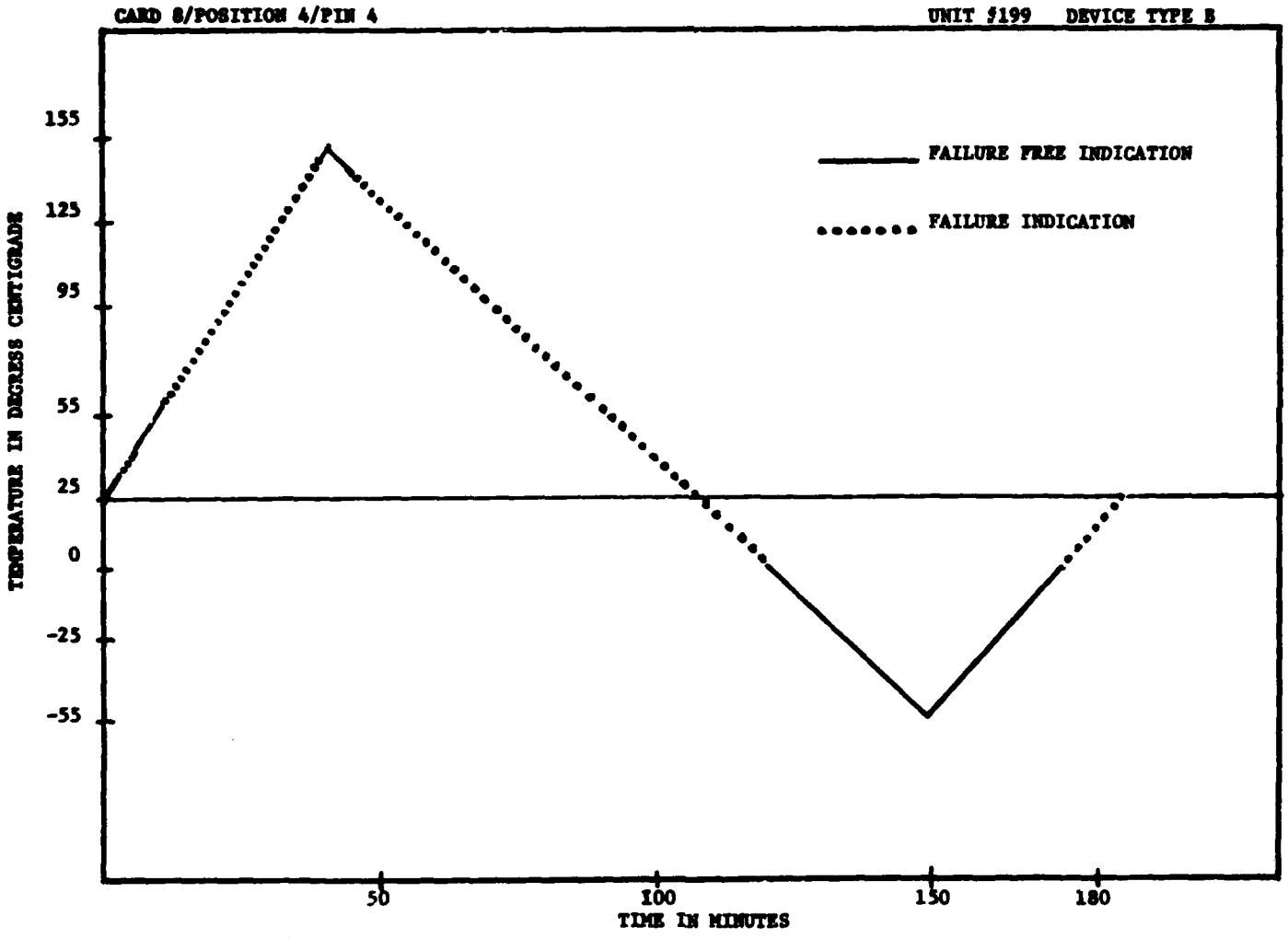


Figure 43 Monitored Temperature Cycle Response - Device 5199, Second Cycle

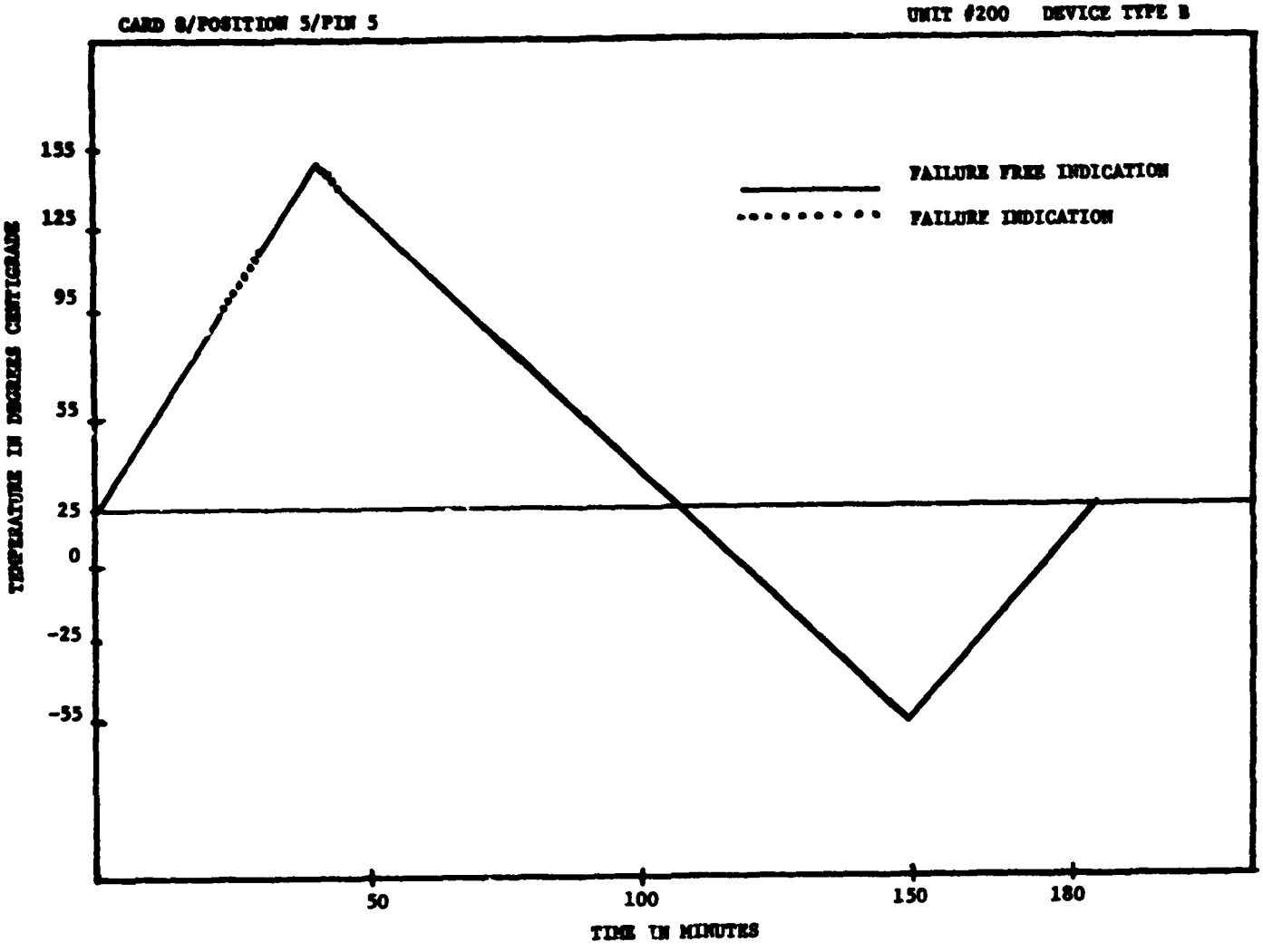


Figure 44 Monitored Temperature Cycle Response - Device 5200, First Cycle

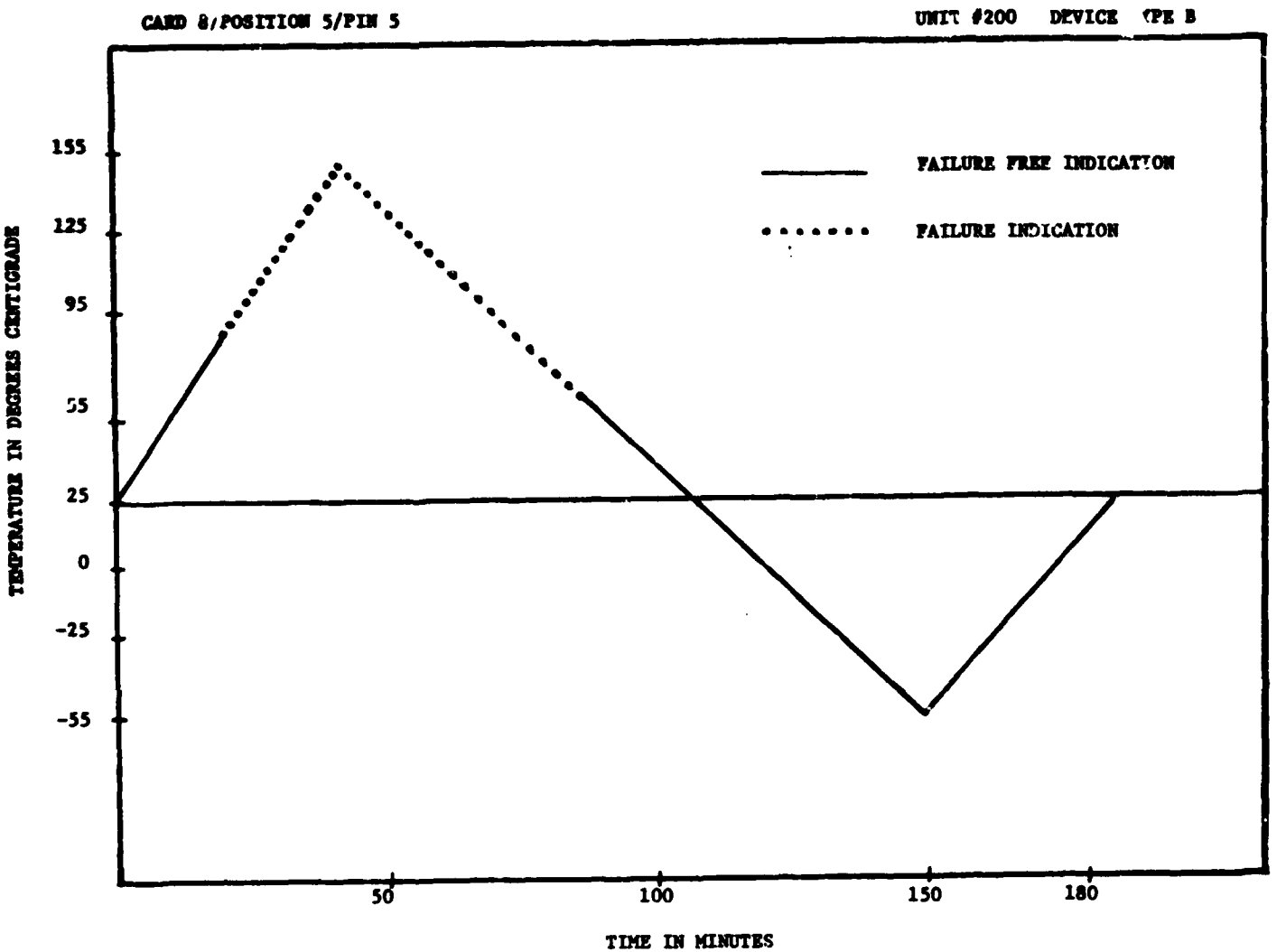


Figure 45 Monitored Temperature Cycle Response - Device 5260, Second Cycle

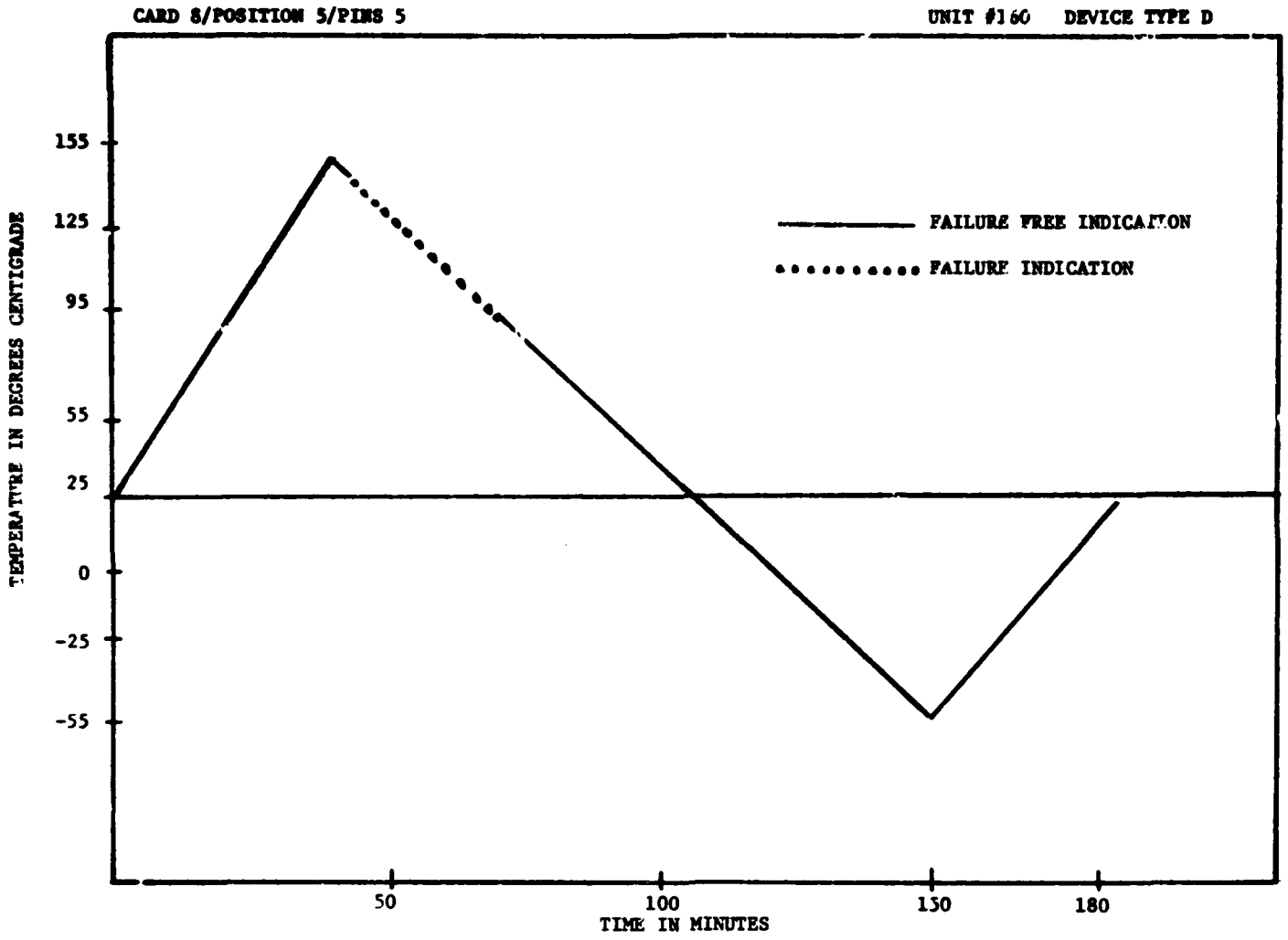


Figure 46 Monitored Temperature Cycle Response - Device 5160, First Cycle

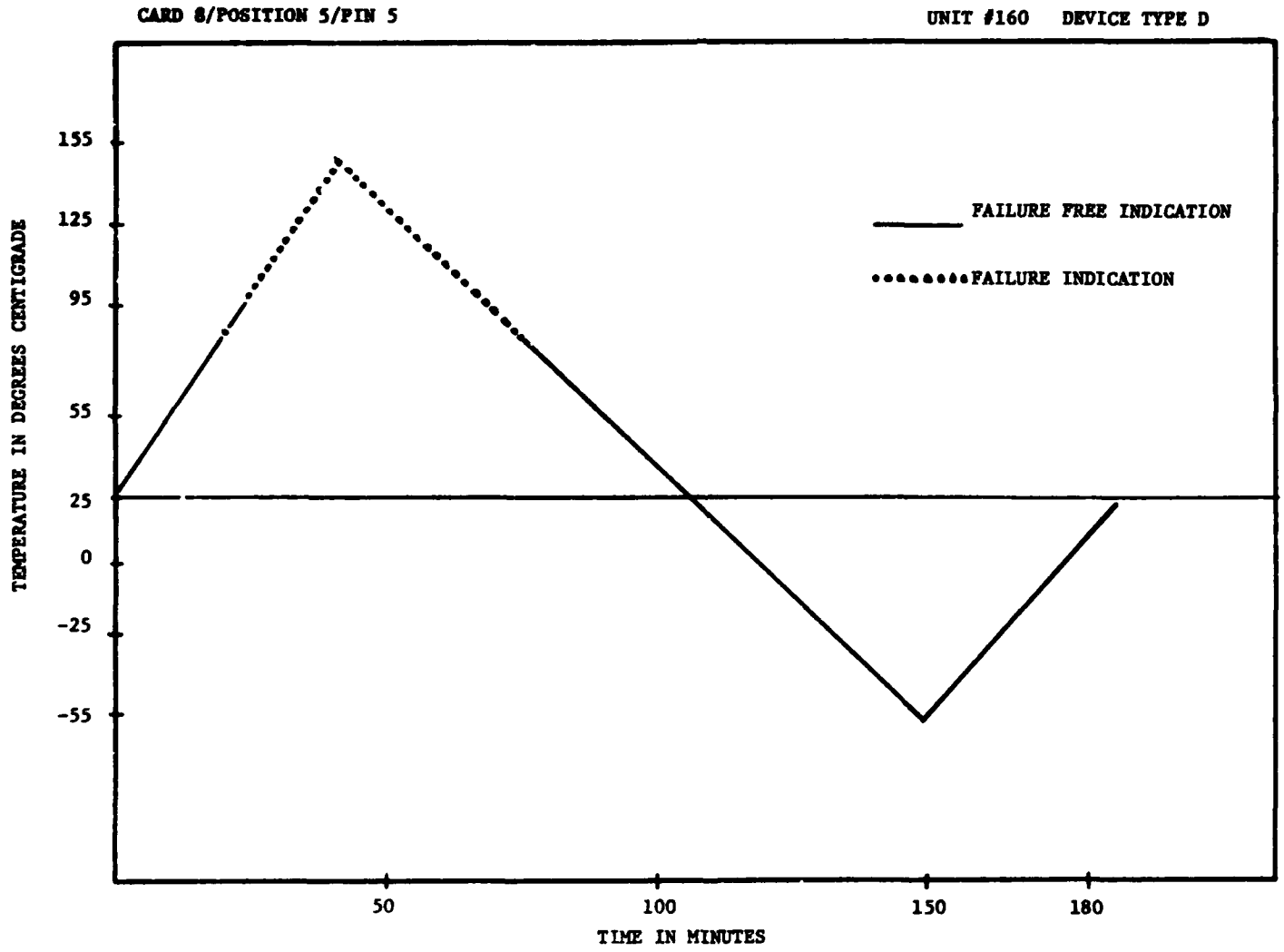


Figure 47 Monitored Temperature Cycle Response - Device 5160, Second Cycle

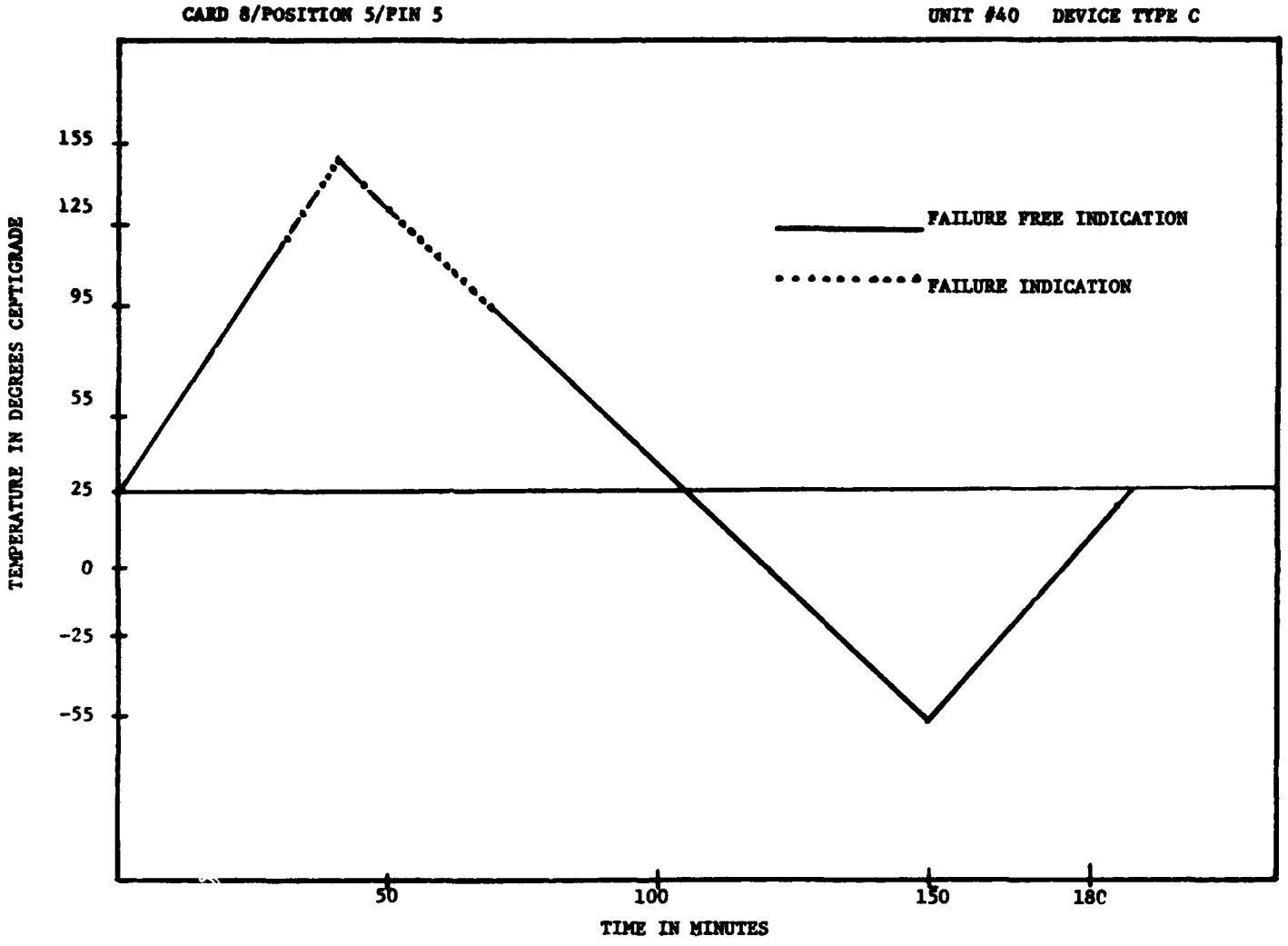


Figure 48 Monitored Temperature Cycle Response - Device 5040, Second Cycle

SECTION V

FAILURE ANALYSIS STUDIES

A. FAILURE ANALYSES WITH THE SCANNING ELECTRON MICROSCOPE

The scanning electron microscope (SEM) was used for detailed analysis of some typical ceramic and plastic encapsulated failures. In this section, results of these analysis are presented to elucidate certain types of failure modes. The SEM is particularly useful in examining small defects such as microcracks, and in analyzing the composition of foreign materials and corrosion products, using the auxilary x-ray equipment.

1. Test Cell 1 Temperature Stress With Bias

Device 1041 This device failed at the 150°C step stress. It was a ceramic packaged device Type A. Preliminary measurements revealed open circuits on all pins but 10 and 11. The case was opened, and examination revealed that all other lead bonds had lifted from the pads. A SEM photograph of one of the bonds is shown in Figure 49. One can see the intermetallic material remaining at the bond site. Note the small area. This was a manufacturing fault rather than a package failure.

Device 1127 This device was taken out of test after the 150°C step stress. It was a ceramic device Type B. Examination of the Teradyne readout showed it actually to be within acceptable limits. It showed acceptable hermeticity on fine and gross leak checks. The case was opened and the circuit

examined with the SEM. There were no apparent anomalies. Figure 50 is a SEM photograph of one of its metal runs, showing modular structure in the metalization.

2. Test Cell 2 Salt Atmosphere

Device 2053 This was a Type A device in a ceramic package. Preliminary examination showed high leakage among all pins, including unused ones. Visual examination showed reddish deposits between pins. The package passed hermeticity tests. The package was opened and examined under the SEM. Numerous examples of corrosion were found. Figures 51 and 52 are two of these. Of special interest is the crystal of sodium chloride on the ball bond in Figure 51. The corrosion on the runs contains aluminum, chlorine, and sodium, probably aluminum chloride and sodium chloride. These products were found inside the package even though it was hermetic prior to this test. Apparently it was open during exposure to salt atmosphere, and the hole corroded shut or was plugged with salt crystals prior to the second leak test.

Device 2055 This ceramic packaged device, Type A, failed leak tests. An SEM examination showed some salt deposits on runs, similar to those shown in Figure 51.

Device 2091 This plastic encapsulated device, Type D, showed severe corrosion on the metalization. Some of this corrosion is shown in Figure 53. Present is aluminum, silicon, chlorine, potassium and calcium. Another instance is shown

in Figure 54 with the previous elements plus gold, tin, iron, chromium and nickel. Aluminum, silicon and gold are, of course, to be expected. The other materials arise from the salt and the pin material.

3. Test Cell 3 Humidity, Temperature Cycling

Results of failure in this cell went very similar to those found in Cells 4 and 5.

4. Test Cell 4 Steam Pressure

Devices 4006, 4007 These were devices in plastic packages, Type C. They showed similar internal corrosion. Corrosion areas in 4006 are shown in Figures 55 and 56. Shown in Figure 55 is material containing copper, sulfur and chlorine. The run integrity is destroyed. Material containing chlorine, copper, and nickel traces is illustrated in Figure 56.

Shown in Figures 57 and 58 is a corroded aluminum run in 4007. The pad has completely vanished. The progress of the corrosion inward is clearly evident. The elements detected are aluminum, chlorine and silicon. Figure 58 is a close-up. In the granular area nearest the pad, the material is much richer in silicon than aluminum. In the flaked area, the converse is true. This results from greater corrosion near the pad removing more aluminum and exposing the silicon substrate.

Device 4130 This was a device in a ceramic package, Type A. Corrosion areas are shown in Figures 59 and 60. The lump on the lead in Figure 59 contains potassium, chlorine and sulfur. The particle in Figure 60 contains iron, calcium and potassium. Other similar deposits were also found as illustrated in Figure 61. This device exhibited open leads.

Device 4066 This was a device in a ceramic package, Type A, that had failed at 1000 hours, but which was left in for the total test run. The case was still hermetically sealed. Opening revealed a fiber on the chip. This was charred and partly decomposed. A picture is sh n in Figure 62. This is clearly a manufacturing defect.

Devices 4163, 4173, 4183 These were devices in ceramic packages, Type B, and all failed similarly exhibiting faults in input offset bias. Only 4173 failed leak test. All showed anamalous characteristics between pins 6 and 10, throwing suspicion on the output stage. The devices were opened and examined. Upon close examination, a crack was found in the metalization of the capacitor, C. In Figures 63, 64 and 65 are views of this crack. Microprobe analysis showed these devices were glassivated and the relative expansion mismatch could lead to this cracking. A crack in the collector metalization of Q20 in 4173 is shown in Figures 66 and 67. The device also exhibited a crack in the capacitor metalization similar to that in 4163. Device 4173 had an hermetic leak, but this probably did not cause the cracking, as other leak-free devices from this cell showed identical faults.

A crack in the collector metalization of Q20 in device 4183 is illustrated in Figure 68.

4. Test Cell 5 Monitored Temperature Cycling

Device 5075 This was a device in a ceramic package, Type A. It failed after 800 hours at 85°C and 85% relative humidity. It had previously experienced 20 temperature cycles. The case was no longer hermetically sealed. An examination with the SEM revealed corrosion products in several areas. Figure 69 is an SEM photograph of Q5. The corrosion products contain potassium, chlorine and sodium as well as aluminum. Shown in Figure 70 is a run near pin 5. The composition is the same as that in Figure 69. The ordered crystals indicate a specific compound. In Figure 71 is a corrosion growth on the edge of the capacitor, containing copper, gold, silicon, sulfur, chlorine (trace),.potassium, calcium, titanium and iron.

Device 5197 This was a device in a ceramic package, Type A. It failed after 1000 hours, but was allowed to remain on test through the 2000 hour period. The case was hermetically sealed. Preliminary checks showed anomalies in the characteristic between pins 6 and 10. The case was opened and an examination performed with an optical microscope. The capacitor metalization was cracked, and the collector metalization of Q20 was cracked.

Shown in Figure 72 is the capacitor and in Figure 73 is Q10. This damage is identical to that suffered by some devices in Cell 4, which were also exposed to prolonged elevated temperature cycles.

5. Test Cell 6 Temperature Cycling and Thermal Shock

The Type B devices analyzed from this test will be treated as a group. Eleven devices were rejected as failures after the thermal shock tests. Most of these devices showed excessive pin-to-pin leakage. After baking for four days at 225°C, all but 6134 recovered. This was opened and examined with the SEM. Figure 74 is an overall view of this device at low magnification. Significantly, this device passed the initial hermiticity test. Figure 75 is a view of 1000 X of one of the deposits. X-ray analysis reveals lead, zinc (trace), iron, silver (trace), silicon and aluminum (trace).

Device 6136, which had recovered after the 4 day bake at 200°C was then examined and found to contain lesser amounts of the same deposits as above. It was also hermetically sealed at testing. In Figures 76 and 77 are examples of the deposits in 6136. The composition is the same as that found in 6134. The glass frit used to seal these devices were probed and found to have the same composition.

Subsequent to these findings, all the 6000 series devices were found to contain similar powdery deposits on the case exterior around the pins. A photograph of this material on 6136 is seen in Figure 78.

It was postulated that the deposit trapped moisture which

caused the inner pin leakage, which was driven off by bakeout. Device 6136 was wet in the pin area and blown dry. The leakage returned. It was removed by a subsequent bake at 200°C for four days.

The glass deposit might have arisen from hot ethylene glycol during thermal shock tests, or during the 200°C bakeout on these devices. To clarify this point, 5199 was subjected to a 200°C bakeout for four days and examined. There was none of the lead deposit. A view of the capacitor metalization is shown in Figure 79. Small modules are seen in the metalization. An enlargement of this is seen in Figure 80. An x-ray analysis shows silicon, aluminum and traces of phosphorus. The metals are to be expected, the phosphorus arises from the glassivation.

This type of nodular formation is common in the Type B devices, and does not seem to be cause for alarm. The conclusion to be drawn is that the liquid-to-liquid thermal shock test is detrimental to the glass frit used in the Type B package. The frit is somewhat soluble in hot ethylene glycol, so that the hot liquid leaches it or decomposes it, subsequently leaving detrimental deposits and in some instances causing hermiticity loss.

This is not, then, a valid method of testing for resistance to thermal shock as it introduces an auxilary failure mode in this particular type package; hence, another type of fluid may be used.

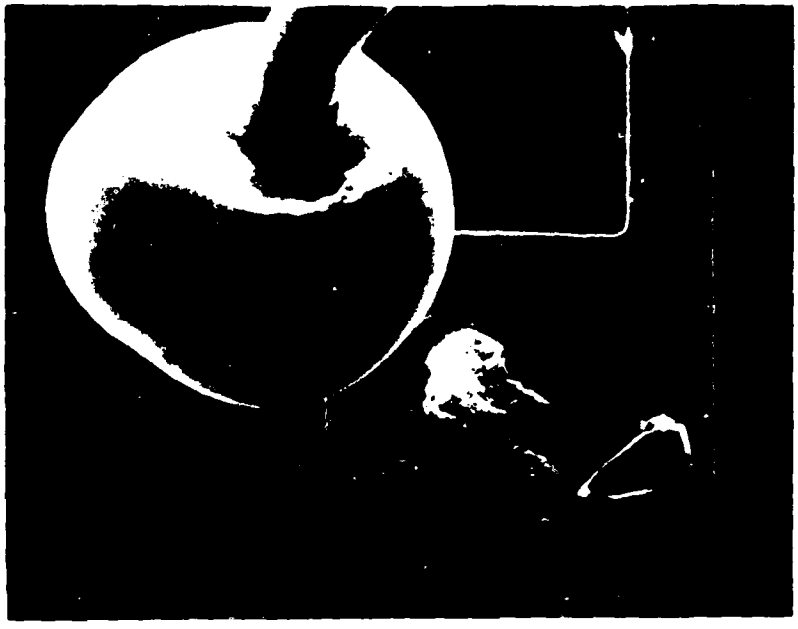


Figure 49 Device 1041 500X

Lifted Ball Bond - Note Small Bond Area - Five Out of Seven Bonds Parted

Figure 50 Device 1127 2000X

Metalization In Good Device

Figure 51 Device 2053 200X

Corrosion Products Containing Sodium, Aluminum and Chlorine

Note Sodium Chloride Crystal On One Ball Bond

Figure 52 Device 2053 500X

Corrosion Products - Aluminum and Chlorine

Figure 53 Device 2091 500X

Lead Corrosion - Foreign Materials Are Chlorine, Potassium and Calcium at Pin 4

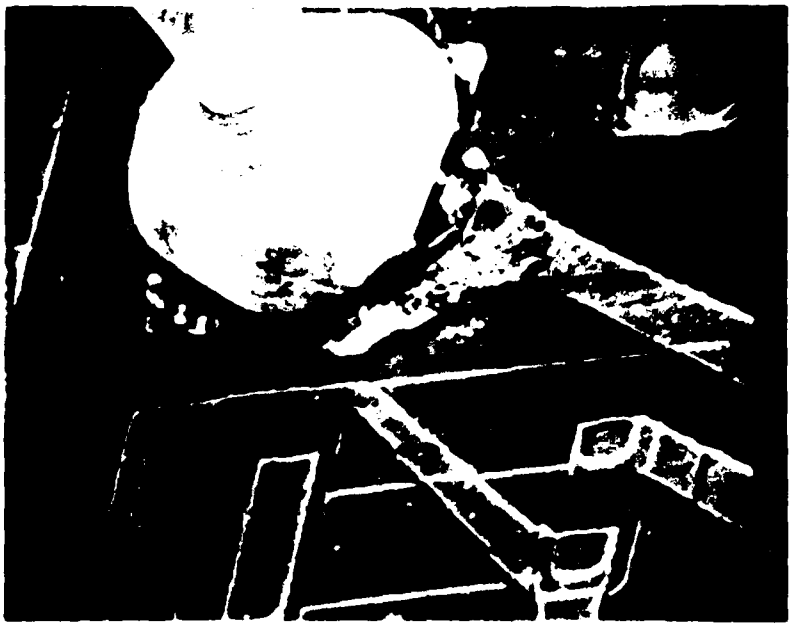


Figure 54 Device 2091 500X

Corrosion - Elements are Chlorine, Tin, Iron, Chromium And Nickel at Pin 5

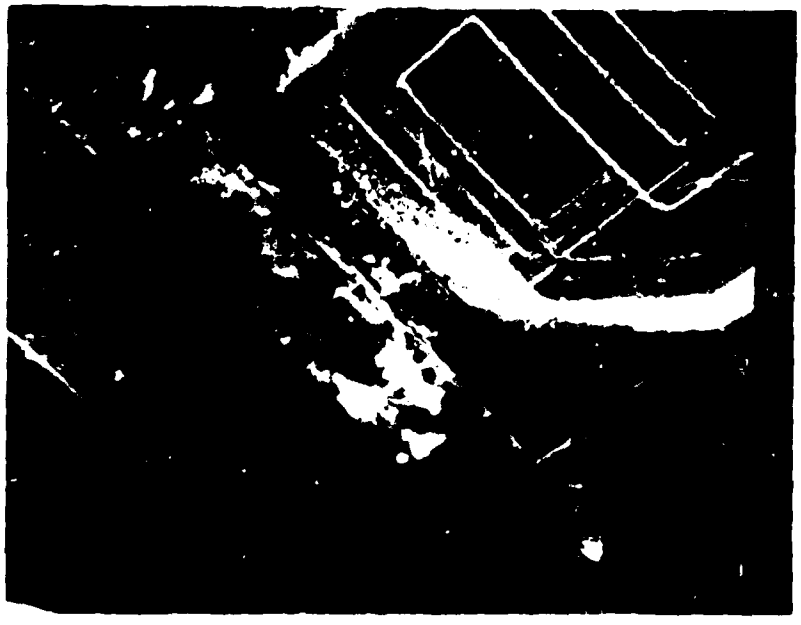


Figure 55 Device 4006 500X

Corrosion Containing Copper, Sulfur and Chlorine

Figure 56 Device 4006 1000X

Corrosion Containing Chlorine, Copper and Nickel Traces

Figure 57 Device 4007 300X

Pad Completely Corroded

Figure 58 Device 4007 1000X

Close Up of Area in Figure 57 Granular Area Poor in Aluminum - Flaky Area Rich in Aluminum

Figure 59 Device 4130 200X

Corrosion On Lead Containing Potassium, Chlorine and Sulfur

Figure 60 Device 4130 1000X

Corrosion Containing Iron, Calcium, Potassium

Figure 61 Device 4130 500X

Corrosion Containing Germanium and Calcuim

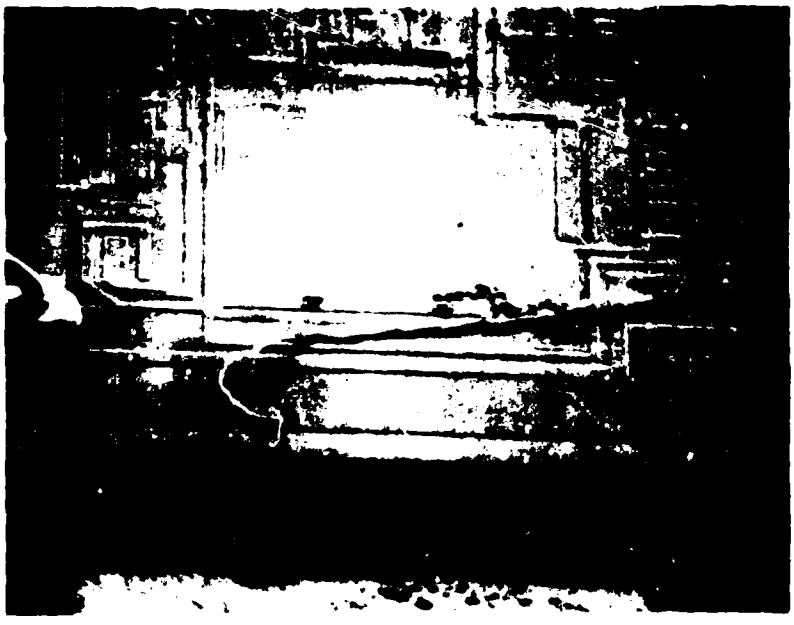


Figure 62 Device 4066 100X

Included Fiber - Manufacturing Defect

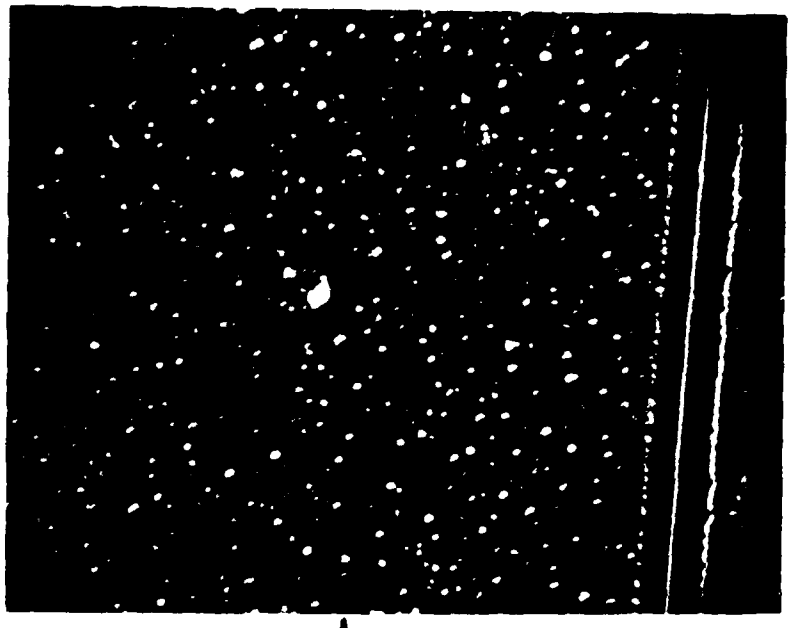


Figure 63 Device 4163 500X

Crack in Capacitor Metalization

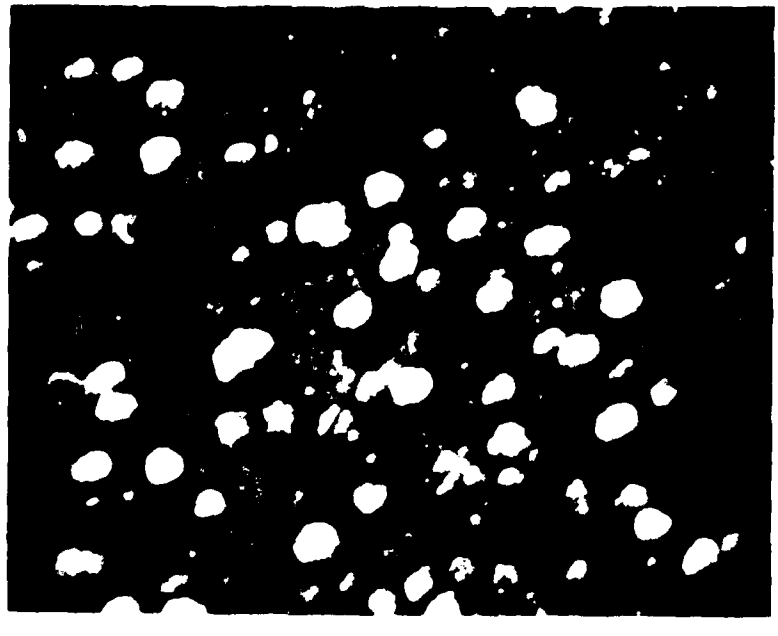


Figure 64 Device 4163 2000X

Same Crack as Figure 63

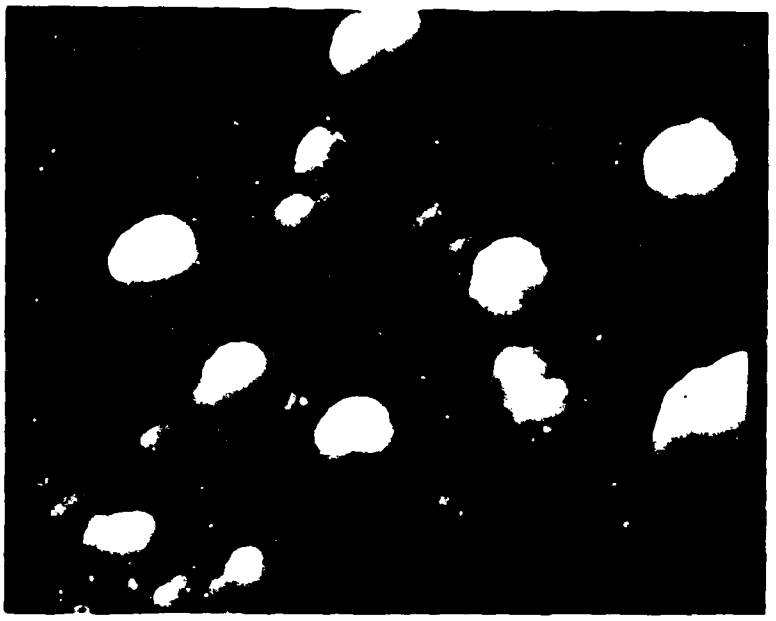


Figure 65 Device 4163 5000X

Same Crack As Figure 63

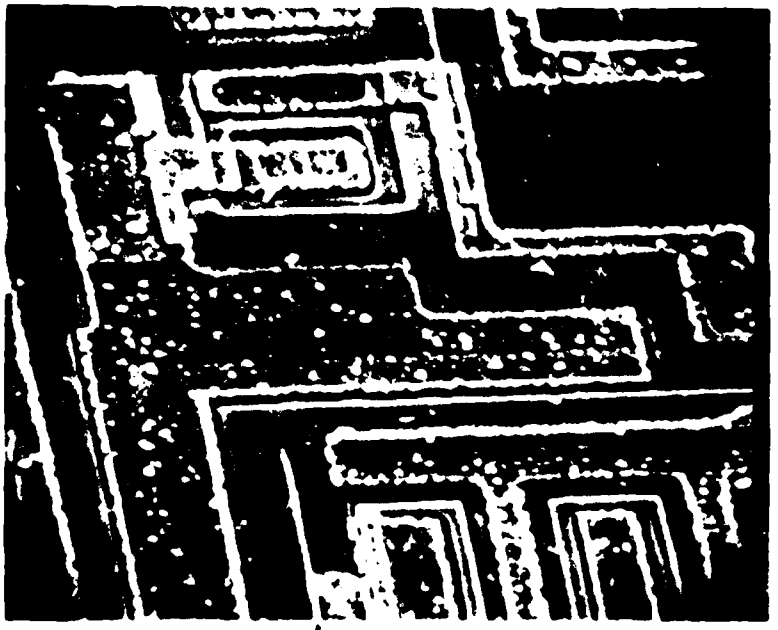


Figure 66 Device 4173 500X

Crack in Collector Metalization, 020

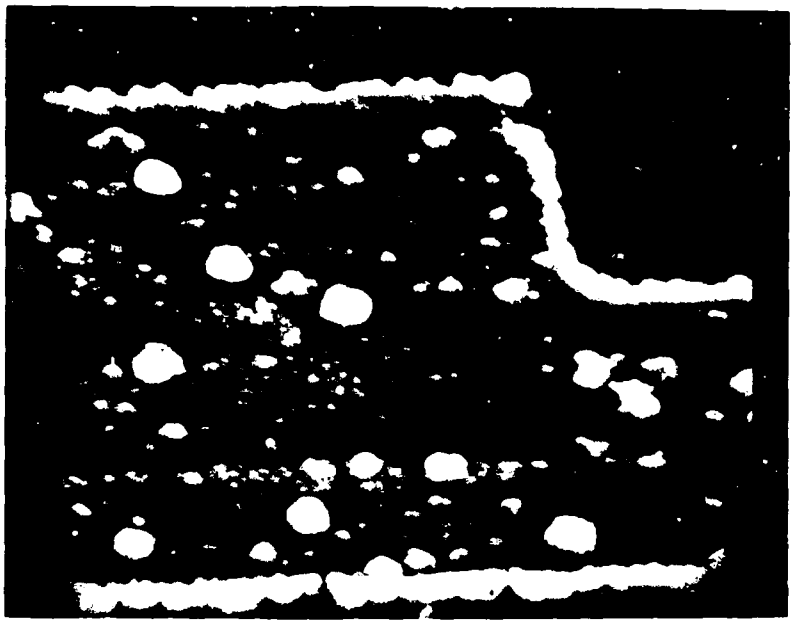


Figure 67 Device 4173 2000X

Same Crack As Figure 66

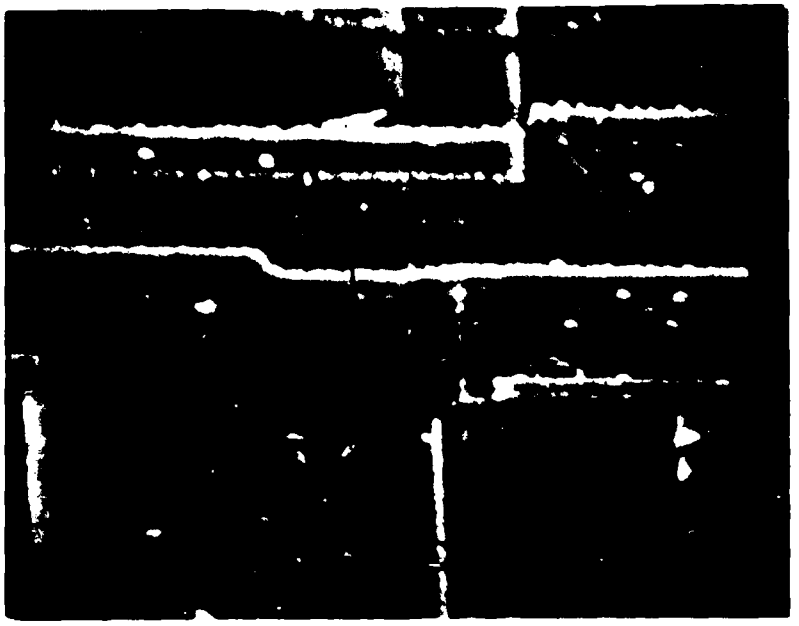


Figure 68 Device 4183 1000X

Collector of Q20

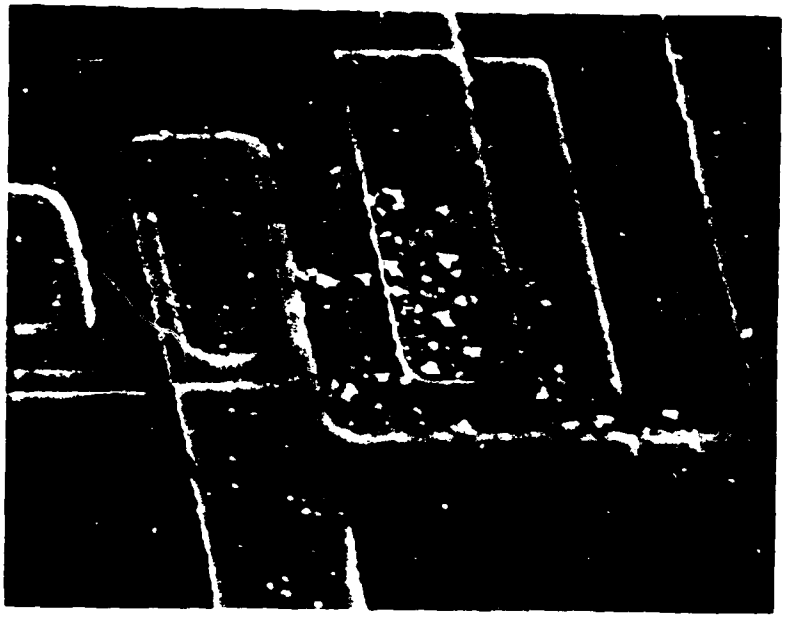


Figure 69 Device 5075 1000X

Corrosion On Q5 Containing Potassium, Chlorine, Sodium and Aluminum

Figure 70 Device 5075 1000X

Corrosion Near Pin 5 - Same Contents as in Figure 69

This is a Specific Compound

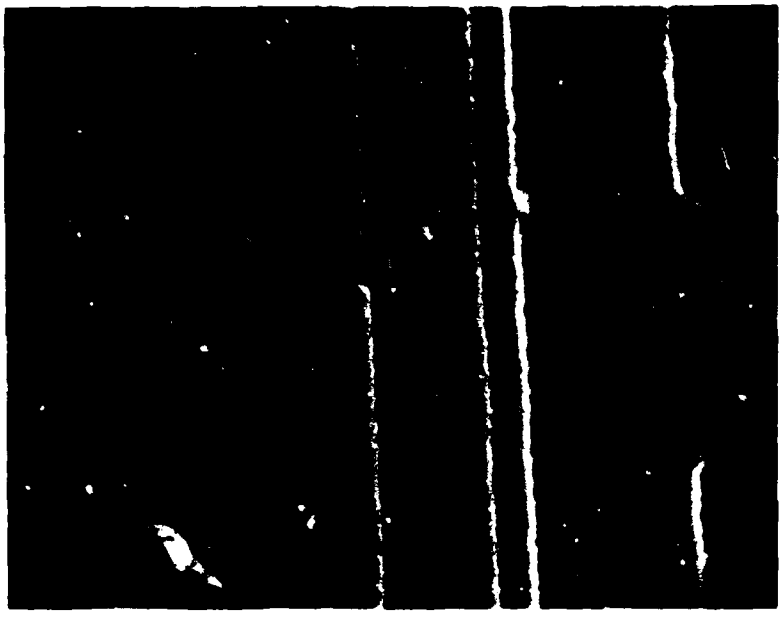


Figure 71 Device 5075 1000X

Corrosion on Capacitor Containing Copper, Gold, Silicon, Sulfur, Chlorine (trace), Potassium, Calcium, Titanium, Iron

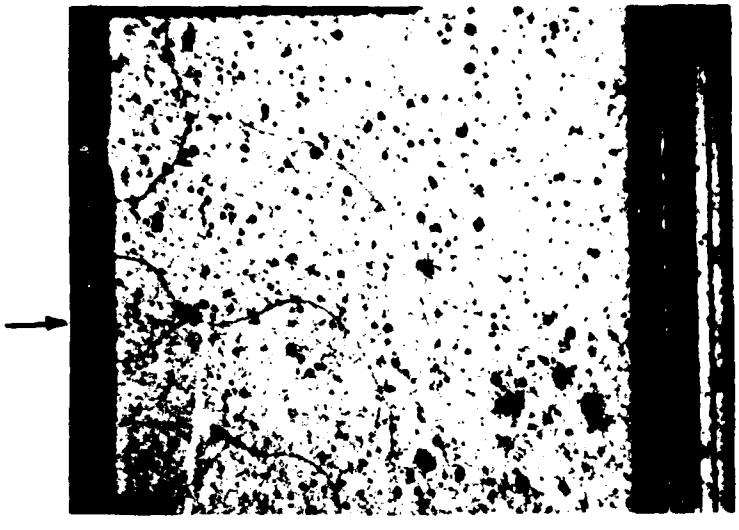


Figure 72 Device 5197

Cracks in Capacitor Metalization

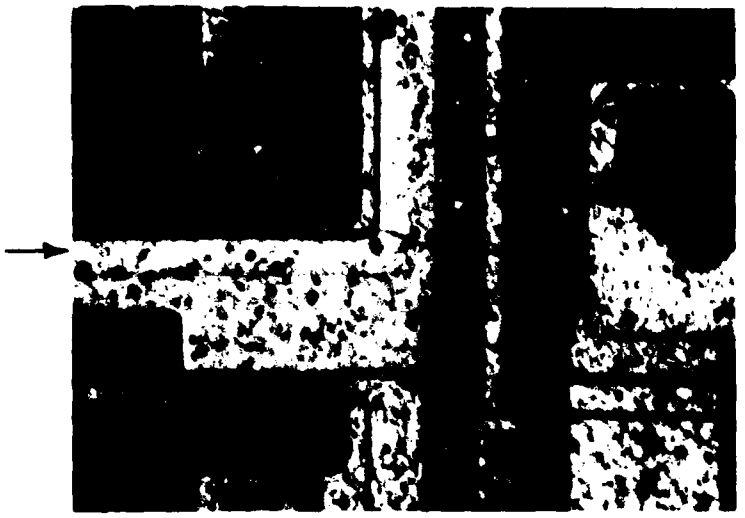


Figure 73 Device 2197

Crack In Collector of Q20

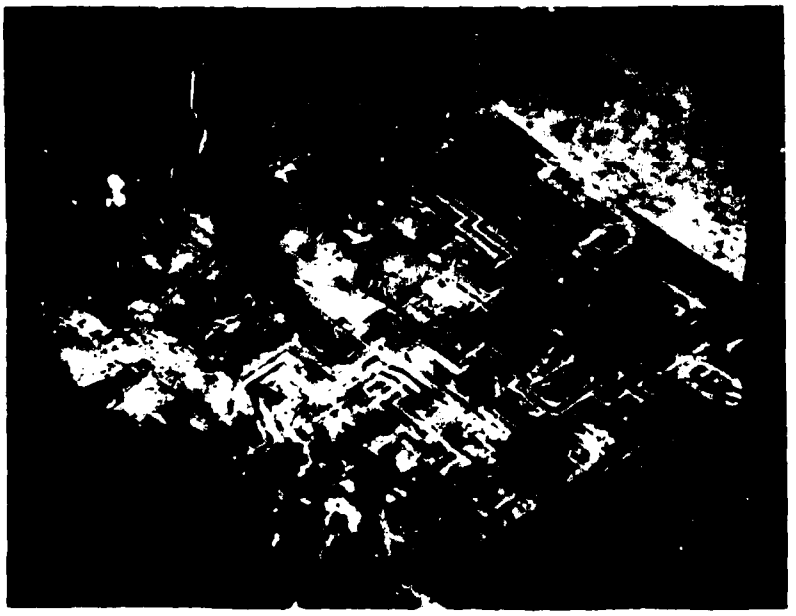


Figure 74 Device 6134 65X

Corrosion Products on Chip Surface

Figure 75 Device 6134 1000X

Enlarged View of Corrosion Deposit Containing Lead, Zinc (trace), Iron, Silver (trace), Silicon and Aluminum

Figure 76 Device 6136 500X

Deposit on Chip Edge

Figure 77 Device 6136 500X

Deposit On Chip Edge

Figure 78 Device 6136 65X

Powdery Deposit on Pins

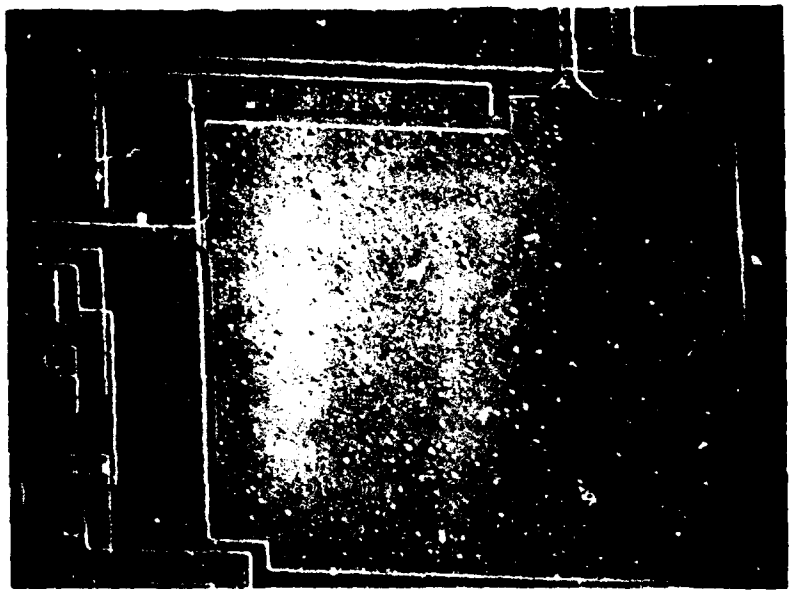


Figure 79 Device 5199 200X

Metal on Capacitor After 200°C 4 Day Bakeout

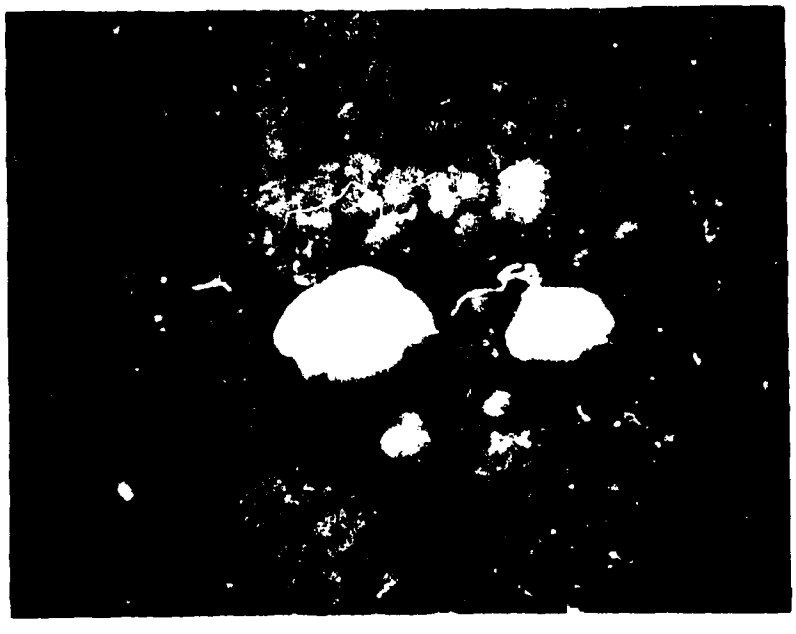


Figure 80 Device 5199 5000X

View of Nodule on Aluminum Contains Aluminum, Silicon, Phosphorus

B. FAILURE ANALYSIS OF PLASTIC ENCAPSULATED DEVICES

1. Test Cell 1 - Temperature Step Stress With Bias

a. Device

Most of the failures received from the temperature step stress with bias series of tests were E Type devices, although the E-Type, made with more sophisticated passivating techniques, were expected to provide improved surface reliability over the C Type. Our analysis of the failed units showed that high leakage was related more to crack defects than to surface inversion. The E Type devices with gang bonded pads had more cracking of critical areas than Type C units. Attached are photomicrographs of several representative failed devices.

1013-C Type, Figure 81 Shown in the photomicrograph is a crack running through the top of the pellet with a short which developed in the center between Pin 11 and Q14 base aluminum runs at the crack. The dark area at the right of the capacitor is the short.

1068-E Type, Figure 82 Shown is the circuit after depotting with all internal copper pin contacts to the circuit undisturbed. The external pins were soldered to impart rigidity to the circuit during depotting. This technique was used for most of the work in this program. In (is an edge crack in the top of the wafer which damaged Q14 transistor. This crack correlates with an unusually degraded characteristic obtained from Pin 11 to 6 (Collector Q14 to substrate).

1061-E Type, Figure 83 The circuit was badly shattered through the outer edge, probably by shock during gangbond as seen at Pin 11 in B.

1063-E Type, Figure 84 This device had an intermittent open at Pin 6 in addition to having electrical degradation. In A of this figure, the copper lead is in its normal position at the pad and a chip-out is visible as shown with the arrow. Strain damage to the silox passivation is seen in the structures above the bond. A deep chip-out damage under the pad is shown in B after the loose copper lead was lifted away.

1064-E Type, Figure 85 The Pin 10 to 6 characteristic, normally that of three forward bias diodes in series with resistance, was degraded to 25 μA at only 0.6 volts. From the schematic, it can be seen that damage to the Q20 PNP transistor can result in this type of degradation.

Shown in A is the Q20 corner of the device, after chemical decapsulation by procedures which cannot damage the silicon or the passivation. The striated lines indicate severe strain in the passivation and a suspected crack is visible under the collector metalization.

In B, a selective silicon etch, i.e., one etching silicon preferentially to SiO_2 resulted in the formation of a deep moat which extended from the lower right corner up through the junctions of Q20. Since it is highly unlikely that crack damage

in the thermally grown oxide covering the junction areas would have extended down only to the silicon surface, the selective etch procedure is postulated to have shown that the junction structures had been cracked in the stress degraded device.

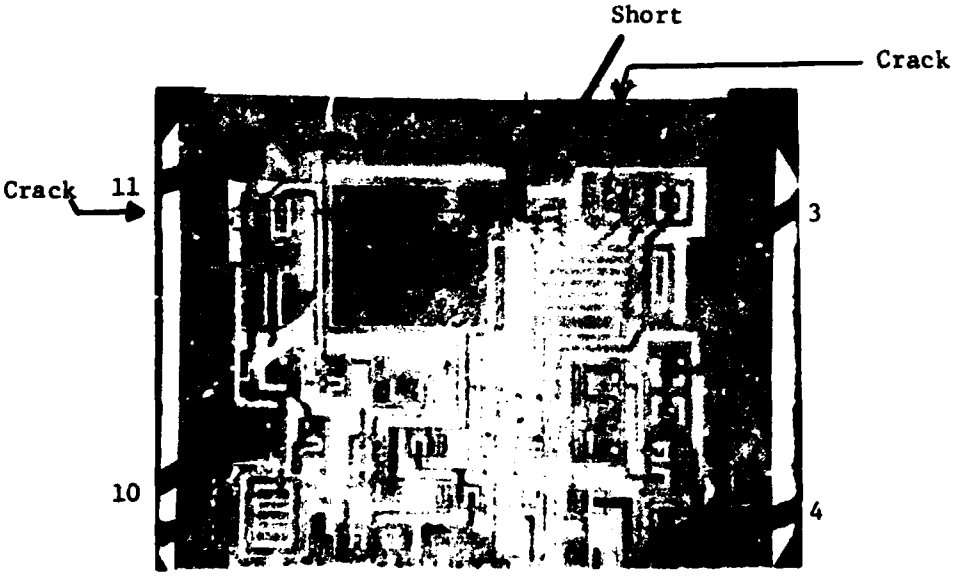
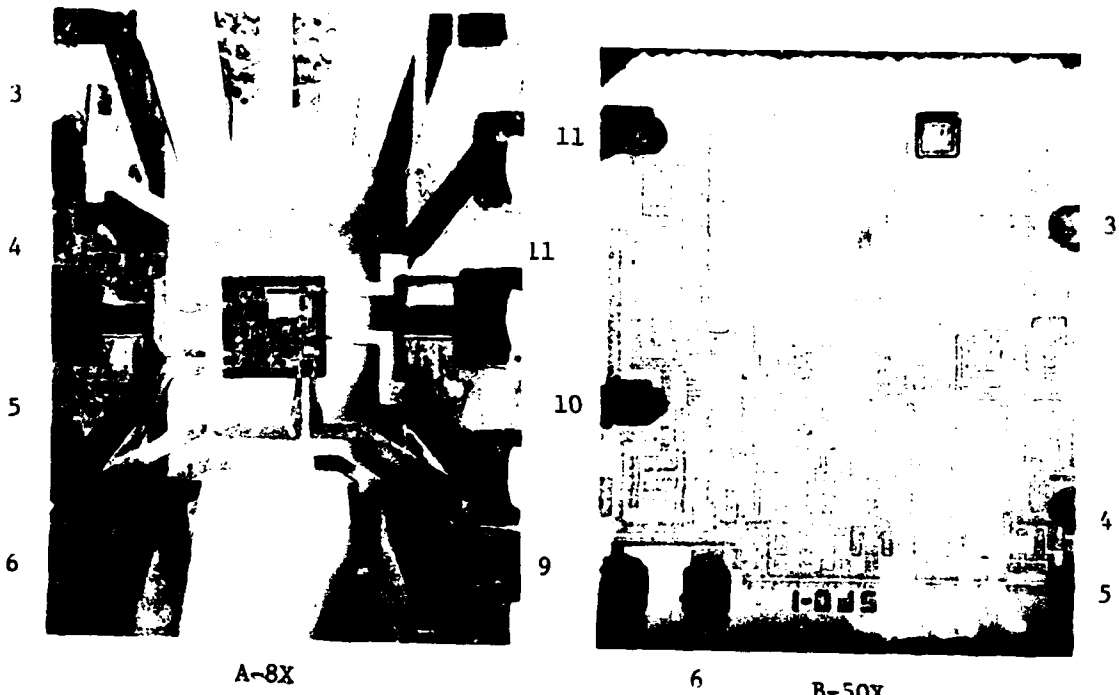


Figure 81 Device 1013 50X



A-8X

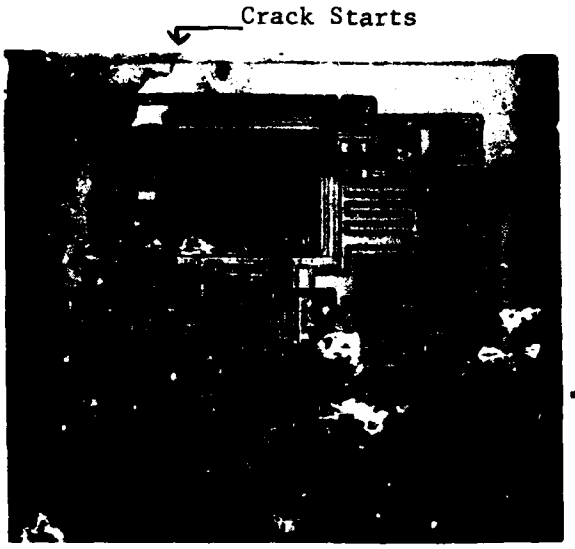
B-50X
As Deposited

Crack Through
Collector Q11

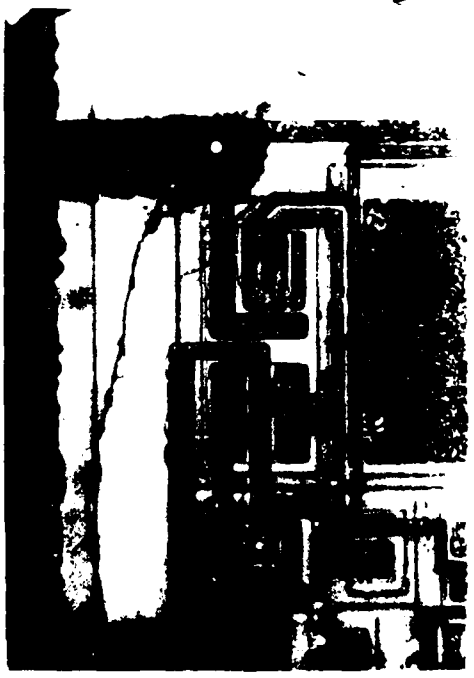
C-100X

Figure 82

Device 1068



A-40X



B-90X

Figure 83 Device 1061

6

A-250X

Bond Pad Fracture

9

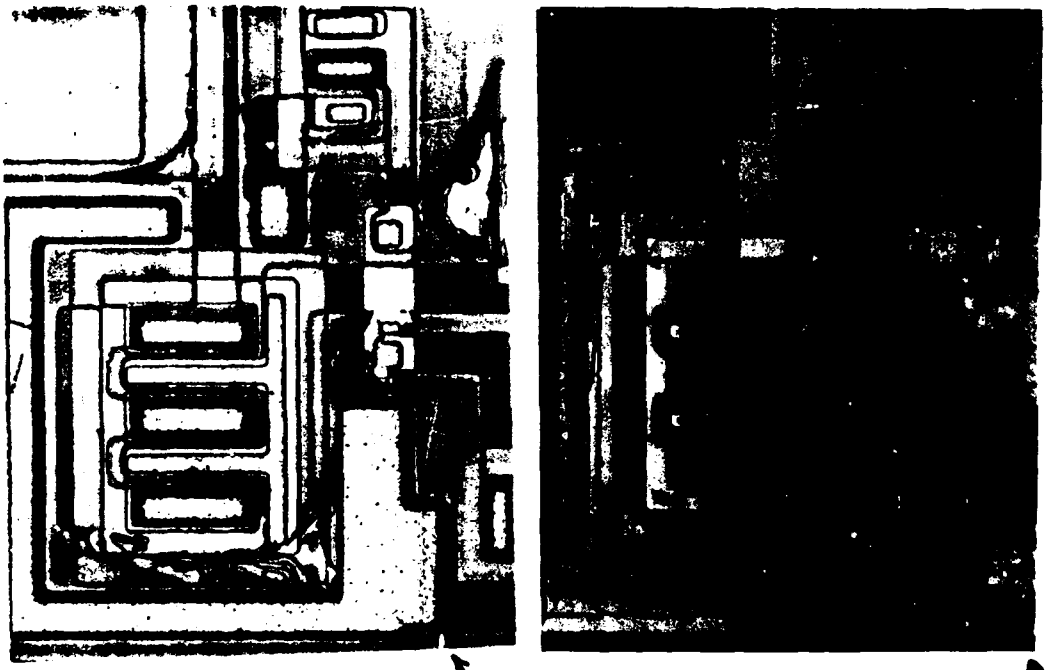
6

B-200X

Copper Lead @ Pin 6
has been Lifted from
the Pad

Figure 84

Device 1063



Crack

Crack which Extended into the Collector Junctions of Q20. The Emitter Junction was also Damaged.

A-228X

B-228X

Figure 85

Device 1064

b. TEGs

Life tests in this group were designed to apply bias across junctions at temperatures sufficiently high to allow ion movement in susceptible structures to induce inversion layers and the high leakage accompanying large changes in surface potentials.

Susceptibility to high leakage is a function of passivation quality as well as the basic design and surface diffusion doping level. If the device is damaged by cracks, this represents the most serious type of passivation defect, since conductive material like H_2O, salts and even contact metal may move directly to the junction surfaces.

Summarized below are electrical characteristics and findings for failed TEG devices. C Type failures were not degraded leakage-wise when received (except for unit #1012) but were defective primarily for open gold-aluminum bond contacts.

E Type devices, made with more sophisticated passivating techniques which were expected to provide improved surface stability, failed due to high leakage in all three TEG transistors in each device. Analysis showed the source of leakage was not due to surface inversion but was more related to mechanical cracking and chipping primarily of the bond pads. This type of failure mode is similar to that also found in the ET devices in stress series 3000. The cracking of silicon under the contact pads is a manufacturing gangbond solder process anomaly.

Cracking of silicon under the collector bond pads of either of the two NPN transistors results in collector conductivity directly to the substrate because of the voltage stress applied from collector to substrate

and this results in degradation of parameters in the damaged transistor as well as in the PNP Q20 of the TEG because of the interconnect system designed into the TEG.

Cracks in the bond pads of the circuits discussed previously could also lead to increased conductivity to the substrate as occurred in Device 1061, Figure 83. Again, the location of the crack and voltages applied across it determine the effect on parameters. For example, fractures in Pad 6 in either the circuit or TEG cannot degrade parameters leakage-wise, as noted in Device 1063, Figure 84, since Pad 6 is already the substrate connection.

Pad fractures caused failures in all TEG failures examined whereas defects and cracks within the circuit itself caused most of the failures in the circuits examined.

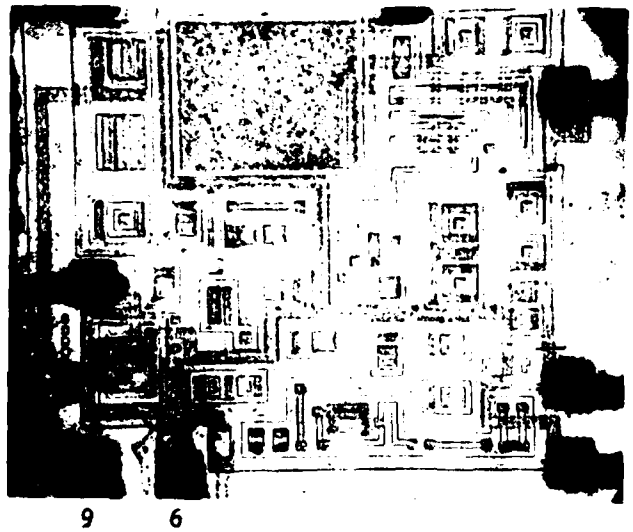
Photos of TEG 1068, Figures 86A-E, were made showing details of the etch procedures used to reveal pad defects hidden or masked behind the massive copper-gold soldered connection at the pad.

Illustrated in Figures 86F, G and H is the degrading effect of one cracked collector pad (3) on the parameters of two transistors (Q2 and Q20). Shown in Figure 86G are the parasitic paths opened by the fractures in both transistors. Reverse characteristics of Q2 and Q20 with the I_{CBO} of each transistor determined by the emitter breakdown of Q2 is shown in Figure 86H. The same type of cracks in Pads 3, 9, 4 and 11 causes high leakage through parasitic paths to degrade Q20.

In Figure 87, pad cracks were found in Pads 3 & 11 of TEG 1079.

Summary - CT Types failed primarily for open gold-aluminum bonds (intermetallic deterioration). ET Types did not develop high leakage due to surface inversion, rather leakage was related to parasitic feedback through defective bond pads.

TEG Unit	Type Construction	Electrical Characteristic	Analysis
1012	CT	Open Pin 4 Degraded Q20	Cracked Pellet & Au-Al open
1016	CT	Open Pin 10	---------- Au-Al open
1026	CT	PL	Recovered Prior to Failure Analysis OK
1036	CT	Open Pin 9	---------- Au-Al open
1065	ET	All Transistors-High CE Leakage	Parasitic Leakage in Cracked Pads
1068	ET	All Transistors-High CE Leakage	Parasitic Leakage in Cracked Pads
1069	ET	All Transistors-High CE Leakage	Parasitic Leakage in Cracked Pads
1079	ET	All Transistors-High CE Leakage	Parasitic Leakage in Cracked Pads
1089	ET	All Transistors-High CE Leakage	Parasitic Leakage in Cracked Pads
1095	ET	All Transistors-High CE Leakage	Parasitic Leakage in Cracked Pads



As Depotted

A-54X

C-100X,Q_2

Gangbonds Etched off in Aqua Regia
Note Defects in Pad 3 in D

B-125X,Q_2

Transistor with Base & Emitter
Gangbonds in Place

Figure 86

TEG 1068

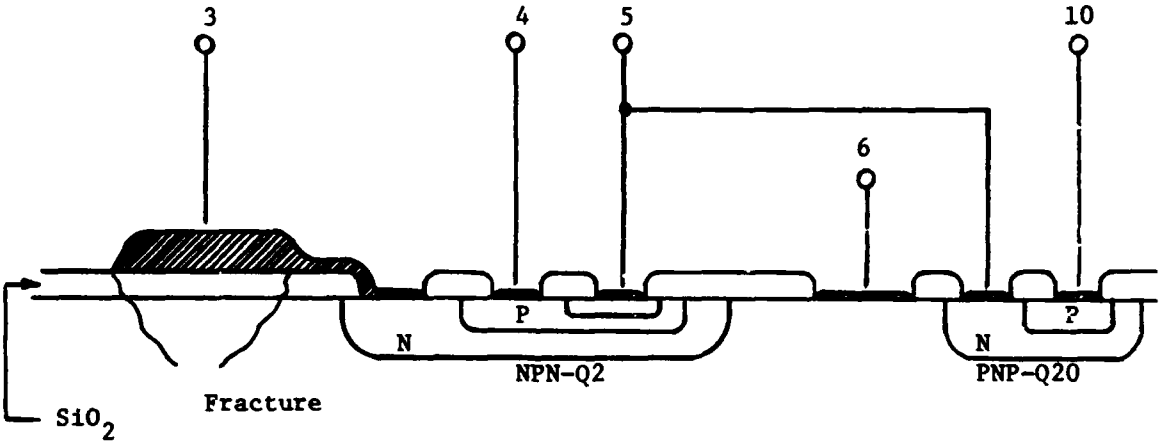
Pad 3
With all Metal Removed by Prolonged
Oxidizing & Aqua Regia Etching
Note Passivation Cracks Appearing
in Areas Previously Covered by Metal

D-300X

Pad 3
With Cracks to Silicon
Enlarged by Selective
Silicon Etch

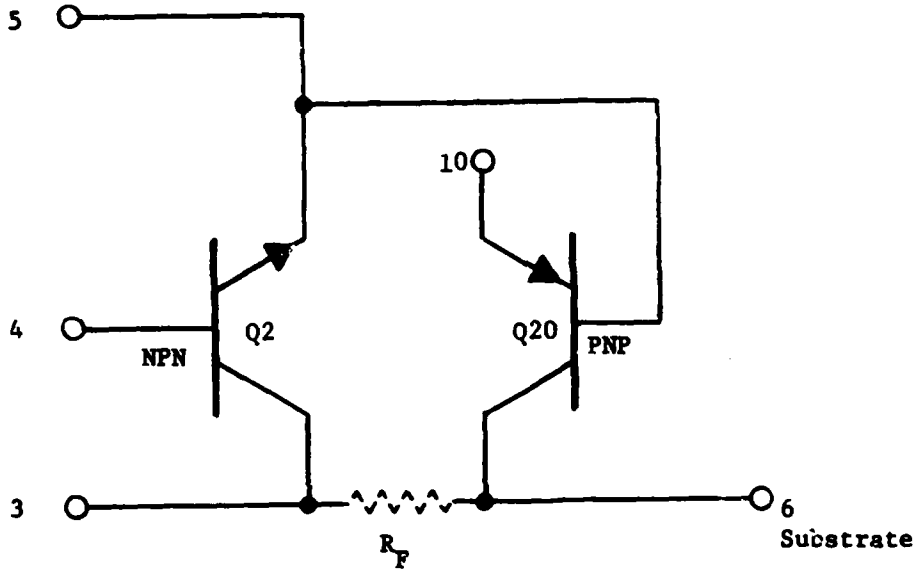
E-300X

Figure 86 TEG 1068 (Continued)



TEG Circuit Cross Section with Fracture Under Pad 3

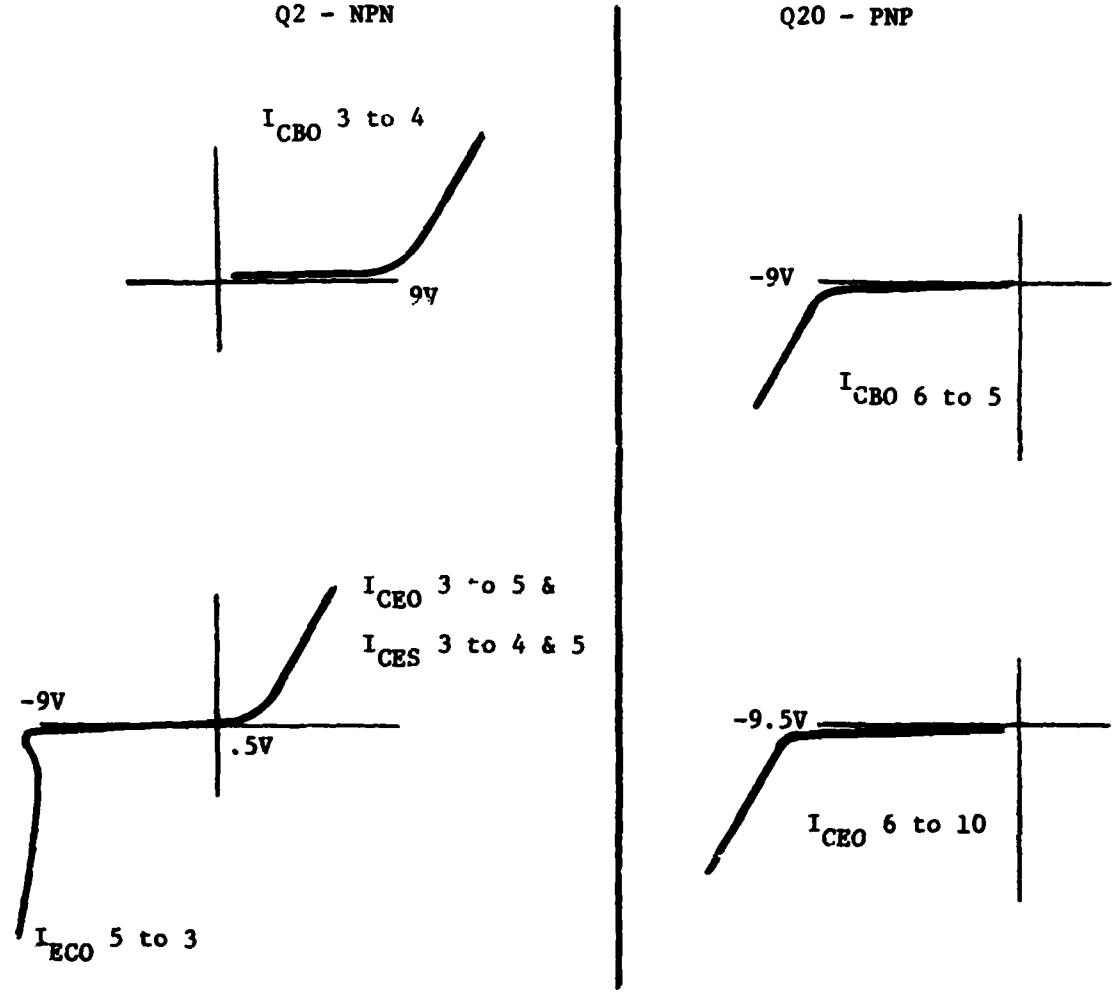
.igure 86F TEG 1068 (Continued)



R_F is the Effective Resistance of the Conductive Path from the Fracture at Pad 3 to the Substrate.

Figure 86G TEG 1068 (Continued)

TEG Reverse Characteristics - Pad Fracture

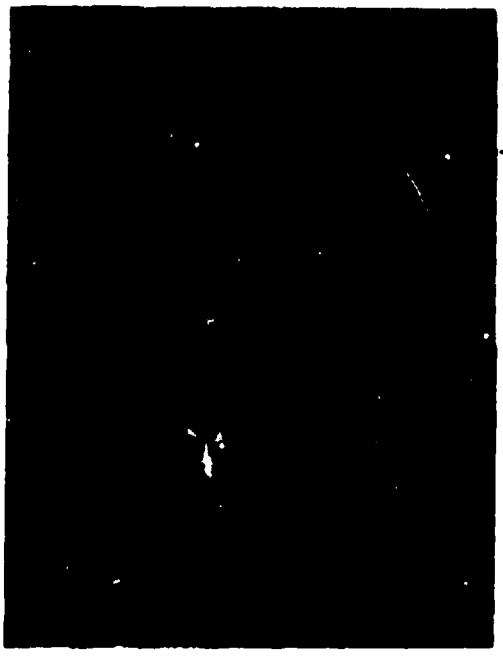


The Breakdown Slopes of I_{CBO}, I_{CEO} & I_{CES} Curves are Determined by the VI Characteristics of R_F - See Figure 86G

Figure 86H TEG 1068 (Continued)

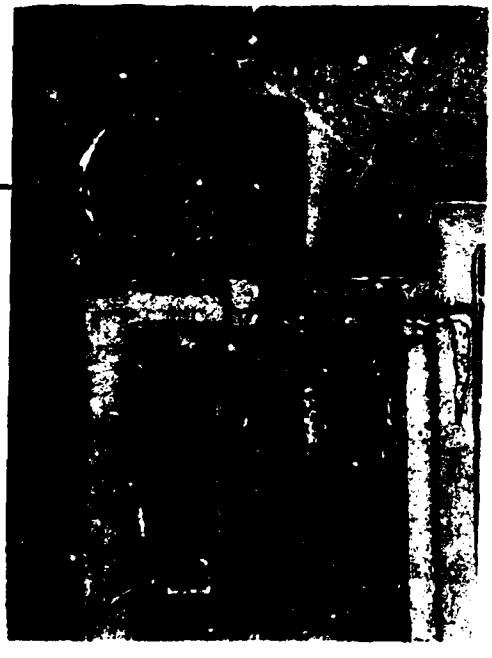
A-144X, Pad 3

View Before Silicon Selective Etch which Shows Fractures Surrounding the Pad



B-228X, Pad 3

After Silicon Selective Etch Note Fractures in Pad 3 & 11



C-228X, Pad 11
Fracture

Figure 87

TEG 1079

2. Test Cell 2 - Salt Atmosphere

Eleven Type D devices, with the following construction features, were analyzed:

- Symmetrical nickel alloy 8 lead headers with gold plated on internal surfaces.
- Silicone rubber barriers on the pellet surfaces.
- Transfer molded silicone package

The eight devices listed all had one or more pins open due to corrosion.

Device	Type	
2091	D	Pins 4 & 5 were open, see Figure 88 & SEM Figures 53 & 54 showing Pin 4 & 5 Corroded Areas
2097	D	Pin 4 was open
2102	D	Pins 5 & 6 were open, see Figure 89 A & B
2113	D	Pins 4 and 5 were open
2106	D	Pins 4 and 5 were open
2109	D	Pins 5, 6 and 9 were open
2110	D	Pin 5 was open
2115	D	Pin 5 was open

Excessive leakage, drifting breakdowns or degradation was not seen in the non-open pins. Depotting showed corrosion destruction of aluminum pads and runs correlating with the electrical characteristic data. There did not appear to be a generalized chemical attack; severe corrosion was confined only to the immediate areas of the open pins.

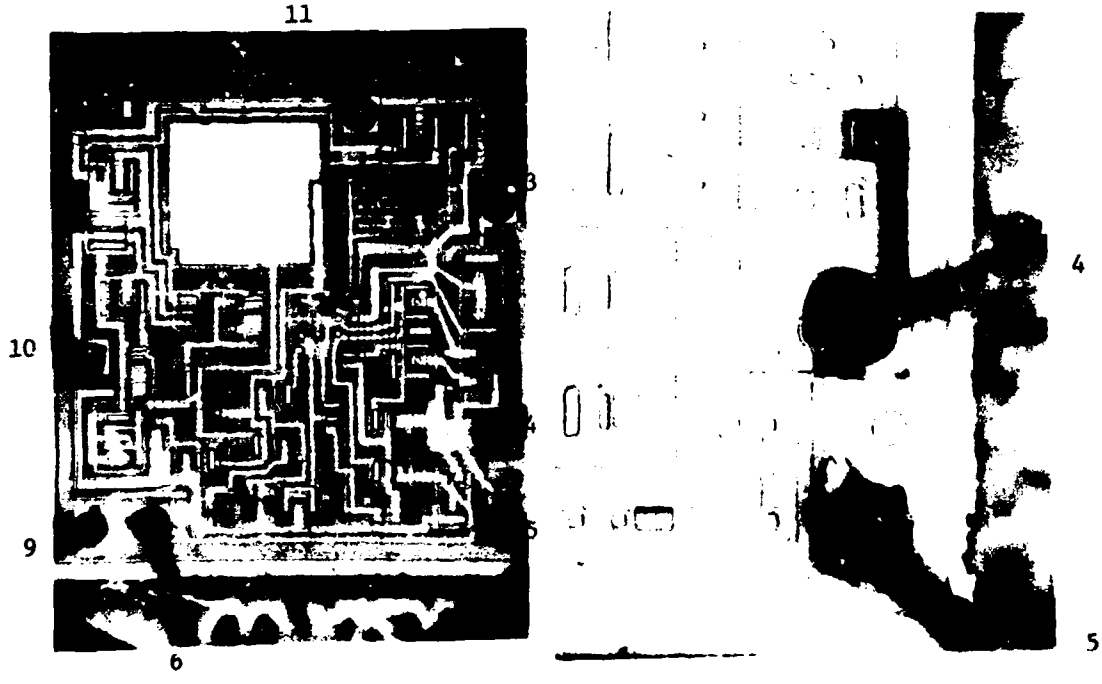
Opens were noted in the aluminum metalization to the pads at Pins 4 and 5 primarily. The package design is such that these sites have the shortest distance to the outside. The absence of corrosion on the pad at Pin 10 which is symmetrically placed opposite to Pins 4 & 5 may be due to the method of device placement in the salt atmosphere

or to some non-symmetry in application of barrier resin during manufacture.

The rapid penetration of salt into the package may be due to the fact that the plastic has siloxane structures similar to that found in quartz or thermally deposited SiO_2, which also has a high permeability to sodium.

The gold-aluminum couple at the bonds is an ideal galvanic corrosion cell in the presence of sodium chloride. The galvanic voltage between these highly dissimilar metals may exceed 3.0 volts and chloride ions promote the solubility of normally insoluble oxidized corrosion products from the anodic aluminum.

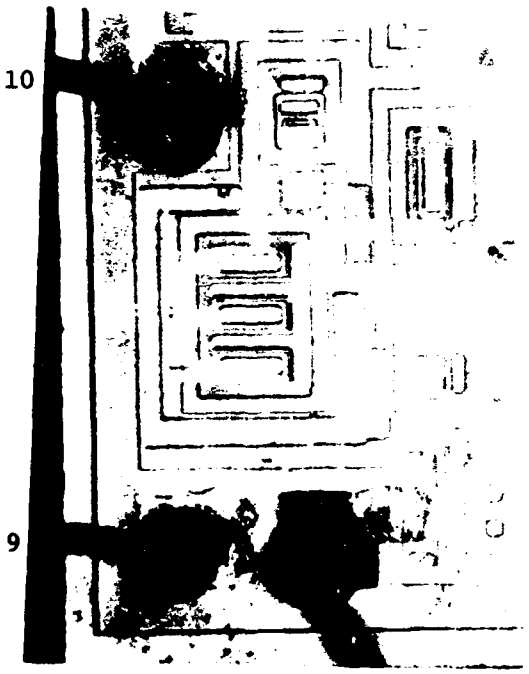
The corrosion rate of aluminum is usually controlled by the rate of diffusion of ions through the protective barrier films of insoluble oxide and hydroxides on the metal surface. The chlorination & partial solution of this film can occur in low pHs and in the presence of chloride ions. Chloride as well as other active ions also increases the conductivity of the liquid film surrounding any corrosion site and thus speeds up the electrolytic ionic exchanges taking place in the corrosion process.



A-51X B-120X

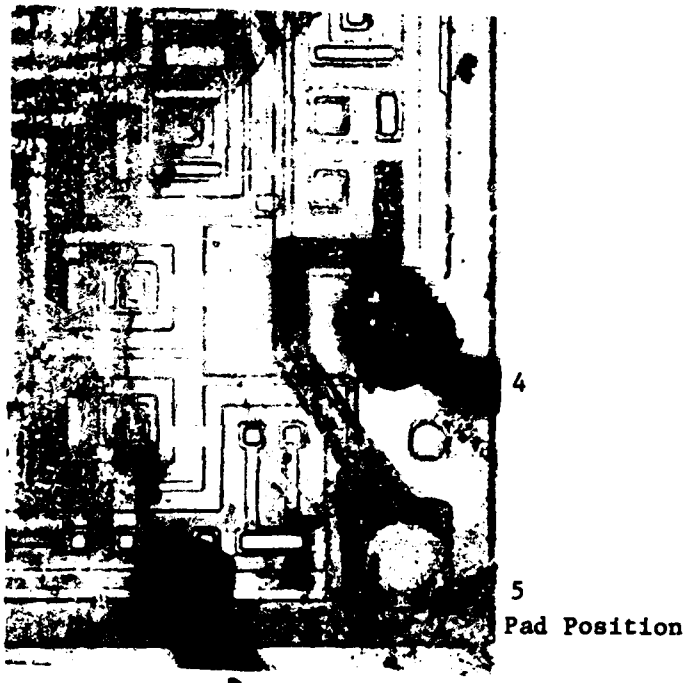
Destructive Corrosion was Limited Only to Pins 4 & 5 Aluminum

Figure 88 Device 2091



A-130X

Corrosion at Pad 6



B-130X

Corroded Open Wire Removed From Pad 5

Figure 89

Device 2102

3. Test Cell 3 - Humidity Temperature Cycling

a. Device

Four Type E devices were analyzed with the following results:

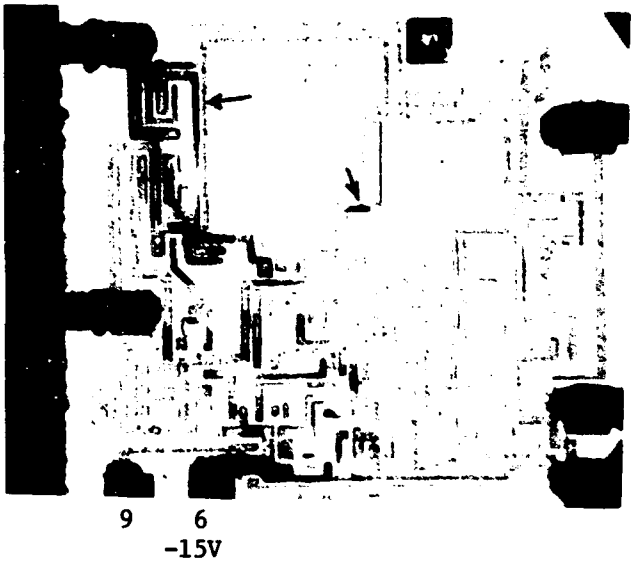
3091, Figure 90 - There was no visual evidence of corrosion damage or penetration of water to the circuit chip. The device had gone into a power runaway from Pins 11 to 6, biased at 30 Volts, with most of the structures between these pins shorted across both active and parasitic junctions. A pinhole short to the substrate at the aluminum run from Q14 emitter could have initiated the runaway.

3094, Figure 91 - Again there was no evidence of corrosion damage or penetration of water. Failure was traced to a 65K Ω leakage path from Pin 5 to 6 (Substrate). The silicon was chipped and damaged at the Pin 5 pad site as shown in the photographs.

3104, Figure 92 - Shorting of Pin 5 to substrate structures was traced to a pinhole in the Silox glass over aluminum runs leading into the Q6 emitter and R2. The R2 structures normally under low bias were thus subjected to the full 15 volts between Pin 5 and substrate (Pin 6). High temperatures developing at the short caused extensive melting at the pinhole contact as well as at the R2 resistor input, as can be seen in B.

3095 - This circuit was removed from life test as a failure. Repeat data taken by the readout area as well as curve tracer readings and stresses in the failure analysis laboratory all indicated the circuit was operational and non-degraded.

The Type E device failures did not occur as a direct result of moisture penetration. Relatively small amounts of moisture may have initiated failures in marginal or defective circuits having cracks or pinholes in their passivation structures.



A-50X

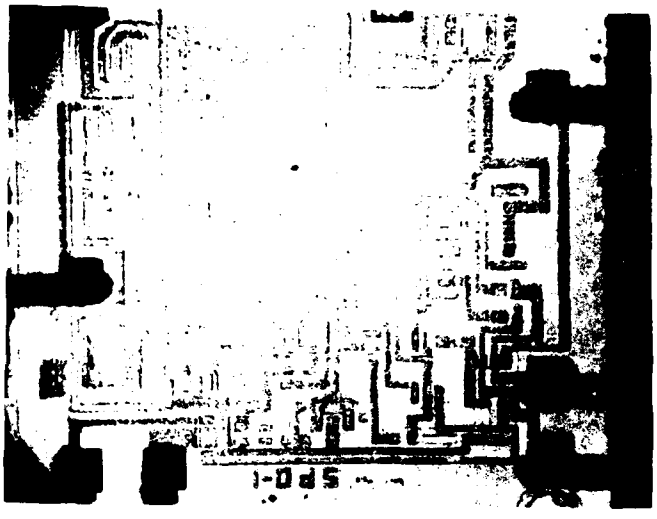
After Etch Removal of Metal Runs

Q14-Aluminum was Shorted into Substrate

B-150X

Figure 90

Device 3091



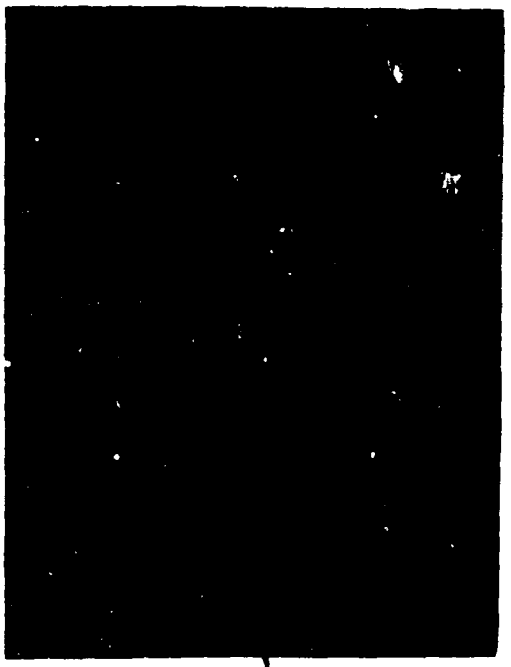
As Depotted

A-50X

A-200X

Magnification of Pin 5 to Substrate Damage Which Developed Conductance Under the Humidity-Bias Stress

Figure 91 Device 3094



Short from Pin 5 to Aluminum Through Silox Glass

A-100X

Pinhole

B-200X

Copper & Gold Bond Pad Structures Removed with Aqua Regia. Arrows Point to Melt Sites at Pinhole and at R2 Input Above.

Figure 92 Device 3104

3. Test Cell 3 - Humidity Temperature Cycling

b. TEGs

CT Types - The primary failure indications in CT type units were opens. As shown below at least 3 of the 6 pins were open while other pins registered anomalous breakdowns indicating that random parasitic rather than normal paths were available for current flow. Analysis showed corrosion of aluminum contacts and runs were the primary failure mechanism.

CT - TEGs

		Failure Indicators	Analysis
3004	Pins Open	#3, 4, 6, 10	Severe Corrosion Attack Especially at Pos. Biased Pins 3 and 9
3005	Pins Open	#3, 4, 9, 10	Severe Corrosion Attack Especially at Pos. Biased Pins 3 and 9
3014	Pins Open	#3, 4, 5	Severe Corrosion Attack - See Figure 93A and B
3055	All Pins Open		Severe Corrosion Attack

ET - TEGs

		h_{FE} @ 5 V & 0.1 mA I_C				
		Q 14		Q 20		
	Failure Indicators	Initial	Final	Initial	Final	Analysis
3074	See Note 1 Below	82	80	28	28	Collector Pad atPin 3 Fractured - Leaking to Substrate
3075	" " "	110	105	22	22	
3079	" " "	62	60	8	8	
3088	" " "	75	65	11	10	
3103	" " "	31	31	8	8	"
3107	" " "	132	130	11	11	"

Note 1 - In all ET Types:

Q2 appeared as CE shorts,

Q14 was virtually undegraded having BV_{CEO} breakdowns greater than 40V,

Q20 was undegraded to voltages of approximately 10 volts at which point resistive breakdown characteristics appeared.

CT Types - Penetration of H_2O followed by electrolytic destruction of the dc biased metal structures on the chip caused failures in CT units. These electrolytic reactions were especially severe where high voltages acted over short distances such as between Pin 9 and 6 structures. Electrical runaway and junction melting may not have taken place in the TEG structures as it did in some circuits under similar environmental conditions because of the current limiting provided by the external 1K resistances in all TEG transistor inputs.

Corrosion and darkening by anodization of positive biased aluminum pads and runs are well understood as oxidation processes leading to the dissolution of the aluminum or to its conversion to insoluble hydrated aluminum oxide depending on the pH and the salts present in the liquid surface films. The presence of salts leached from the epoxy or carried in by the penetrating water tends to accelerate these anodic destructive reactions at Pin 9, 3, or 5 structures as shown in Figure 93A of TEG 3014.

Negative or cathodic biasing is not effective in protecting aluminum from corrosion as it is with other metals like iron. This is primarily due to the increase in pH around the cathode at high current densities which then results in chemical attack of the amphoteric metal. Thus Pin 6 and Pin 10 structures located close to Pin 9 were attacked also.

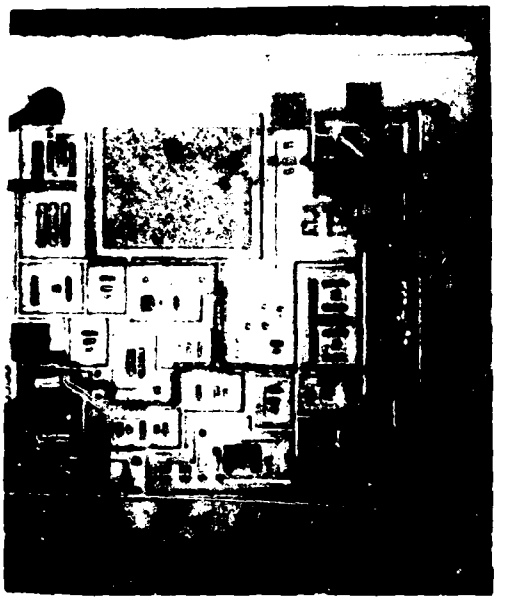
Gold is usually corrosion resistant and insoluble. However, in the strong positive fields at the Pin 9 and 3 wire bonds in Unit 3014, gold solution and transfer took place with redeposit of the dissolved metal on negative cathodic surfaces such as the unpassivated edge of the substrate. This transfer of gold indicates chloride ions were probably present in the penetrating liquid films. See Figure 93B. This is the only device with gold migration observed in this program.

ET Types - Leakage degradation in all six ET type devices was very consistent and completely different from CT type devices. As shown in the summary, there were no opens. Q14 leakage was relatively undegraded while Q2 and Q20 were consistently degraded as indicated by characteristics noted in the summary. Analysis showed these characteristics were due to silicon fracturi , in Bond Pad #3, the collector input of Q2 transistor in all 6 devices examined.

ET Types - Current Gain - Due to extremely high I_{CEO} leakage, Q2 h_{FE} was not evaluated. However, Q14 and Q20 transistors at 2 volts were undegraded in I_{CEO} and h_{FE} measurements showed excellent gain stability, although the emitter junctions had been under a 3 volt reverse bias throughout the stress. This bias presents a field which drives mobile ions in the passivation in such a way as to deplete the base surface. h_{FE} is a more sensitive detector for changes in the base surface potential than I_{EBO}. Stability in h_{FE} is, thus, an indicator that mobile ion density in the oxide is relatively low, a conclusion also arrived at from the fact that I_{CBO} failures were not due to surface effects, but rather to damage of the bulk silicon.

ET Types - No destructive attack of aluminum was noted in these units. The CE shorting of Q2 was traced to cracks induced by faulty processing under the collector input of Q2 - Pin 3. Conductive paths will develop across cracked structures or junctions much more readily than across

undamaged passivated structures. As a result, low levels of H_2O penetration with bias resulted in conduction to the substrate and the characteristics noted previously. This is the same type of damage noted in ET-TEG devices failing the Temperature Step Stress with Bias (1000 series). See Figure 86A through H for a physical as well as a circuit description of the failure mode. The consistent occurrence of damage at Pin 3 points to a gang bond assembly fault for a group of units during fabrication. During gang bonding, an unequal distribution of heat can result in the defective pin solder melting last. The total force of the bonding tool as well as some rocking motion is then transferred to Pin 3 and a fracture could occur. In Figure 94, a typical Pin 3 bond fracture is revealed in TEG 3075 after etching off the bond pad metal. During analysis of TEGs the degrading effect of the Pin 3 fractured pad could be removed by scribing open the long aluminum interconnect between the base of Q20 and the emitter of Q2.



Severe Corrosion at 3, 4, 5, and 9

A-50X

Pin 9-6 Area - Arrows show Gold Deposited on Negatively Biased Areas - Pin 6 Aluminum

B-140X

Figure 93 TEG 3014

Fracture of Silicon at Bond Pad #3-After Aqua Regia Removal of Metal on the Pad

Figure 94 375X TEG 3075

4. Test Cell 4 - Steam Pressure For Forty-Eight Hours Followed by 85°-85% Humidity Life with Bias

Fourteen of the circuits received from this stress included 7C, 2D and 5E type devices and were analyzed as summarized below:

	Type	Failure Indicator	Failure Analysis
4001	C	Pin 11 Open	Pin 11 (+15V input) corroded open
4002	C	" " "	" "
4003	C	" " "	" "
4006	C	" " "	" " See Figures 95A, 55 & 56
4007	C	" " "	" " See Figures 95B, 57 & 58
4019	C	" " "	" "
4038	C	" " "	" "
4130	D	Recovered prior to F.A.	Parameters may have degraded temporarily from H_2O permeation then recovered
4145	D	Circuit problem from Pin 11 to 6	A damaged run from Q11 to R5 opened by electromigration compounded possibly by corrosion See Figure 96B
4083	E	B+ (Pin 11) input shorted to output (Pin 10)	Pin 11 to 10 circuit structures zapped across active and parasitic junctions Pin 7 was ok
4084	E	B+ shorted to substrate (Pin 6). Pin 10 output was open	Circuit was destroyed by massive runaway or latch-up Pin 7 was also shorted to 6
4085	E	Completely shorted	" " " " " " See Figure 97 for an xray enlargement
4089	E	Completely shorted	All internal structures including copper inner leads to the outer frame were destroyed by massive runaway including Pin 7

	Type	Failure Indicator	Failure Analysis
4090	E	Pin 11 to 6 had an anomalous high voltage breakdown	Aluminum run from Pin 11 to Q13 was found open as well as some small patches of missing aluminum in Capacitor caused by corrosion through Silox pinholes.

C Types - A common failure indicator in the C Type devices was an open Pin 11. Depotting of several units showed similar causes of failure as in C types subjected to other bias humiditylife test stresses. Aluminum runs and pads were darkened or anodized to some degree throughout the circuit but with no complete isolation or destruction of continuity except in the Pin 11 area, biased at +15 volts. Here, severe anodic attack occurred isolating the Pin 11 input and damaging neighboring structures such as Q14. No latch-up or runaway occurred in these devices, failure was only by electro-chemical damage to contact metal structures due to penetration of moisture. The unusually large number of C type devices failing is due in part to the high pressure drive-in of moisture prior to start of the 1000 hr life test.

D Types - One of the D Type failures, 4145, had anomalous curve tracer characteristics indicating a probable circuit run open from Pin 11 to 6, while the other device 4130 appeared to have recovered Bakeout of both devices failed to change parameters. Upon depotting, we found an aluminum run from Q11 to R5 to be corroded open at one small site. See Figure 96B for Device 4145. The aluminum at all other sites in both devices appeared to be in excellent condition. It is believed that a localized manufacturing anomaly left a very small aluminum cross-section which opened up by electromigration or by a relatively small amount of corrosion in the

presence of some moisture which had penetrated to the aluminum during the biased humidity life test.

E Types - Three of the E Types submitted for failure analysis (4084, 4085 & 4089) had shorts which developed from Pin 7 to 6. Pin 7, a copper run adjacent to 6 was not connected to the circuit but had been biased at +15 volts in order to test for phenomena such as metal migration across the plastic surfaces under humidity. Shown in Figure 97 is Device 4085 in which the copper run at Pin 7 is partially destroyed by conduction from Pin 7 to 6 with continuity maintained by a mass of carbonized plastic formed within the device by the intense runaway condition. Circuit connected gang bonded leads were also found to be electrically damaged by runaway in Circuit 4089. This positive response thus indicates that moisture penetration to isolated leads in these devices had initiated a destructive conduction mechanism external to the chip and massive enough to be visible in xrays.

In the chip, active and parasitic junctions located between Pins 11 & 6, the B+ to B- inputs biased at 30 volts, were also extensively zapped in the three devices having copper lead damage as well as in Device 4083 which had no evident lead damage external to the chip. The damage in Device 3091 Figure 90 is also typical for E type devices in this stress series. Device 4090 had not been zapped. A slight amount of corrosion damage was found, apparently due to penetration of moisture through Silox pinholes. One of these small area corrosion sites opened an aluminum run leading from Pin 11. No evidence was found of any extensive corrosion damage in the aluminum metalization of other E type chips depotted for study on this program. This contrasts very markedly with C type chips in which aluminum damage, especially at anodic areas, was very heavy.

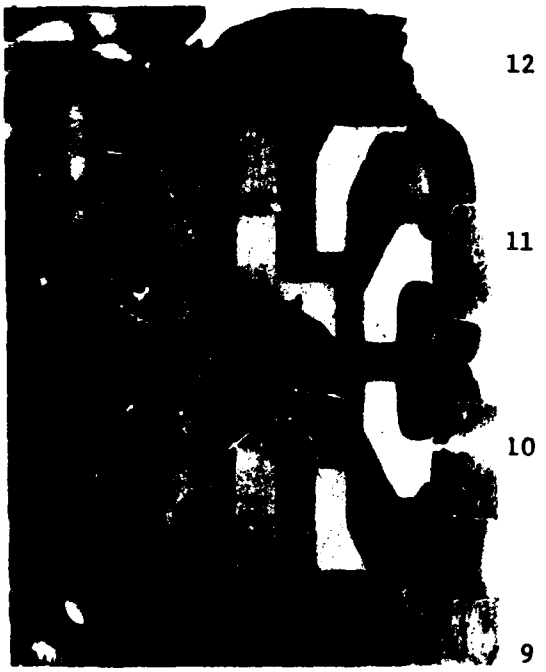
In summary, the passivation coatings on the E chip was more effective

in protecting aluminum from corrosion than the C system. However, a destructive latch-up or thermal runaway mechanism caused failures in E type units. No latch up type failures were found in C type units although water penetration to the pellet conductors was obviously greater and more extensive. Thus, moisture penetration to critical areas cannot account for the zaps found only in E type devices. A complete explanation of this phenomena would require further investigations.

A ~ 110X

B- 110X

Figure 95 Devices 4006, 4007



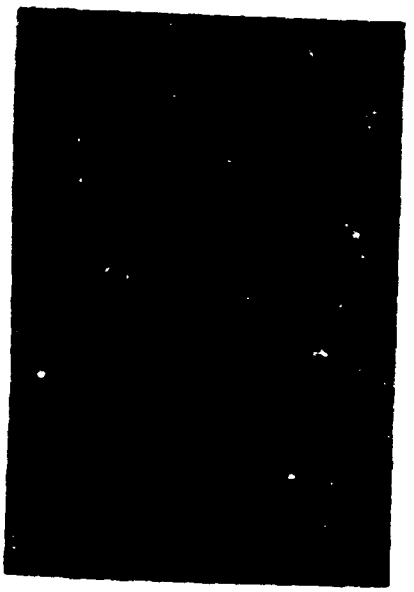
A-10X - As Depotted

R5

B-270X
Note Break in Aluminum Run From Q11 to R5

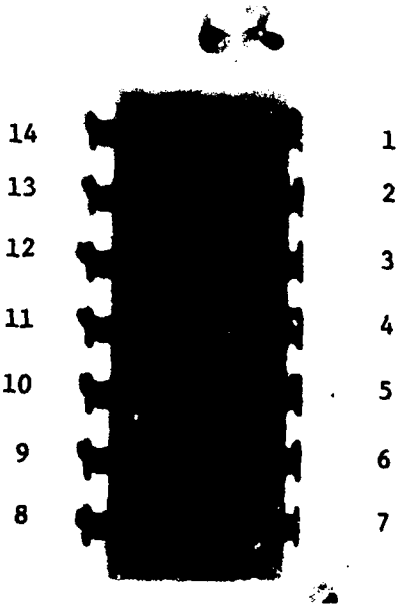
Figure 96 Device 4145

X-ray Enlargements



Device 4085 - Destroyed by Electrical Overload; Note Pin 7 Damaged

A - 3.7X



Control - Normal Unit

B - 3.7X

Figure 97

Device 4085

5. Test Cell 5 - Monitored Temperature Cycling Followed by 85°-85% Humidity Life with Bias

Five C Type devices analyzed in this series were subjected to a temperature cycling sequence which included a sensitive monitor screen (MTC) for detection of intermittent or open bonds. The pin positions of all defect readings were recorded but the devices themselves were continued on to 1000 hours of humidity and bias life testing with no failure analysis at this stage. Parameter measurements made at zero hours for these defective units failed to confirm any opens previously detected. After completion of the life test, four of the devices which had failed the latter stress were submitted to failure analysis as well as one device, 5033, which passed all parameter tests even after completion of the humidity bias life test.

Since the MTC indicator of failures had not been confirmed by subsequent repeated measurements, a prime purpose of failure analysis was to determine if these original failure indicators were correct. Failure analysis was made difficult by the fact that water penetration and corrosion can cause well made adherent bonds to open and continuous aluminum structures to open up. This type of damage can completely over shadow and mask any weakness originally detected at the suspect site. See 5010 in Figure 98B analysis as an example of this condition in which connections to pads at 6, 9 and 10 opened during depotting. The pad at 11 failed during the humidity and bias life testing as shown in Figure 98A.

Our analysis showed that the probability, that MTC intermittent indicators were correct, was greater than 50% in three of the five circuits. Yet in all devices, failure by opens was not detected at the MTC suspect pins, which showed no sign of intermittence during repeated circuit parameter tests or even in failure analysis measurements designed to detect intermit-

tence. Failure in four units was due entirely to severe anodic destruction of aluminum in the vicinity of Pin 11, biased at +.5 Volts during the life test.

The intermittent MTC sites are believed to have been "healed" during testing by a phenomenum more common in plastic encapsulated devices than in non plastic hermetics. When a bias is applied across a closely spaced void, the high field may cause dielectric breakdown or arc-over which leaves a conductive path of carbonized plastic or rewelded metal to maintain continuity. In hermetic devices without plastic overlays aluminum runs are almost never successfully re-estsblished by this means while gold aluminum bonds isolated by Kirkendall void formations, may be readily healed. These bonds, however, are sometimes mechanically weak without a surrounding plastic support and can be re-opened with shock or vibration. A good example of a true open, with continuity detected only by MTC, which opened again with the plastic removed is in Pin 5 of Device 5023 shown in Figure 99B. An example of the cause of life test failure is shown at Pin 11 in Figure 99A.

This self-healing property in plastic devices may be of advantage in maintaining operation in a working circuit if an open develops as a result of electro migration. However, initial detection of opens and failure analysis is difficult. Analysis of results of the five MTC identified device failures is summarized below:

Device	MTC Pin Intermittent	Cause for Failure in Life Test	Analysis of MTC indicated Pins
5010	9	Pin 11 destroyed - generalized corrosion	50% probability that Pin 9 bond adhesion had been defective originally. - Figure 98
5016	9	Pin 11 destroyed - slight amounts of generalized corrosion	MTC indication was faulty. Pin 9 continuity was non-defective See Figure 100

Device	MTC Pin Intermittent	Cause for Failure in Life Test	Analysis of MTC Indicated Pins
5023	5	Pin 11 destroyed - slight amounts of generalized corrosion	MTC ind. was correct. An open was found in Pin 5 aluminum. See Figure 99
5039	3, 11	Pin 11 destroyed - slight amounts of generalized corrosion	Evidence @ Pin 11 was destroyed There was a high probability that the MTC Pin 3 reading was correct.
5033	3	No failure detected in life test measurement	High probability that the MTC Pin 3 reading was correct

Technique for Checking Continuity at MTC Indicated Intermittent Opens Pins.

Continuity checks after depotting are advantageous because carbonized paths and dielectric breakdown sites which may have bridged open contacts with relatively non-intermittent low resistance paths are removed by the depotting process. See an example of this in 5023 shown in Figure 99B. Prior to depotting all external leads are soldered together as the most reliable method for holding all internal contacts in position without movement during the decapsulation process. Corrosion weakened, but not open, contacts are especially fragile. Device 5016, which had an MTC indicated intermittent at Pin 9 is shown in Figure 100. After depotting, all gold wire connections to the external copper header leads are checked for continuity and then they are pried loose. Retention of bonds to the chip pads indicates good mechanical adhesion but not necessarily good electrical continuity. An insulating teflon strip is then slid under the gold wire that was connected to the lead frame and a probe check is made directly from the wire to the substrate or to aluminum patterns on the chip. Good electrical conductivity at this stage indicates the bond probably had not been intermittant prior to humidity life testing.

Five of the E Type devices that failed on humidity life test were analyzed. Failure in four devices was due to circuit overload or latchup from Pin 11 to 6, biased at +15 and -15 volts respectively. Q14 transistor adjacent to the Pin 11 input is usually completely shorted out during the overload, see 5087 in Figure 101. The overload to Pin 6 can proceed by one of several paths via Q14, 15 and 22 or more round-about via Q12 and Q7. Device 5097 was overloaded to an extreme degree.

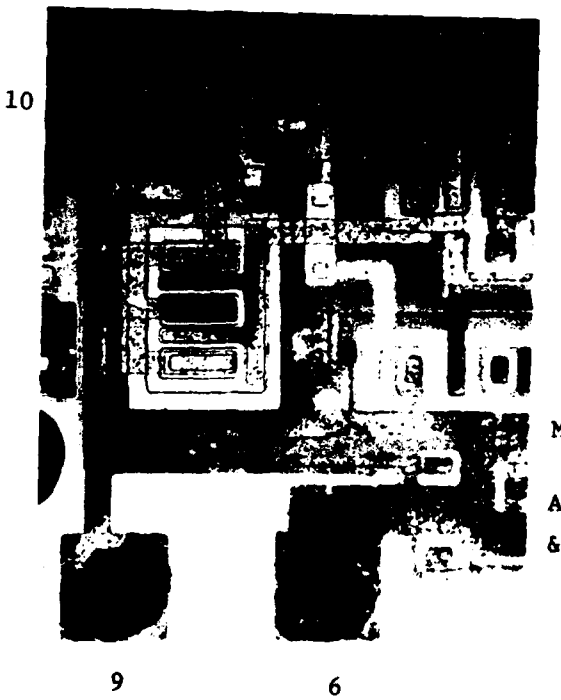
There was no evidence of aluminum corrosion in Type E units which had failed by electrical overload or latch-up. The Type E passivation is a more effective barrier to water permeation than the silicone rubber used in Type C packaging. Just as with units subjected to the stress series of Cell 4 water penetration to critical areas alone does not account for the onset of latch-up or runaway since Type C devices were penetrated by water to a larger degree but did not latch-up.

The results of failure analysis of these five E Type devices are shown below:

Electrical Overload Path	Failure Analysis
5087 - Zap from Pin 11-6	Latch-up but no evidence of internal corrosion
5092 - " " "	" " " "
5095 - " " "	" " " "
5097 - " " "	" " " "
5115 - Device checked good upon receipt for failure analysis.	

A-135X

Pad 11
Anodic Corrosion from
Life Test Stress



B-135X

MTC Indicated Open
Pin 9

Appearance of Pins 10
& 6 is Similar to Pin 9

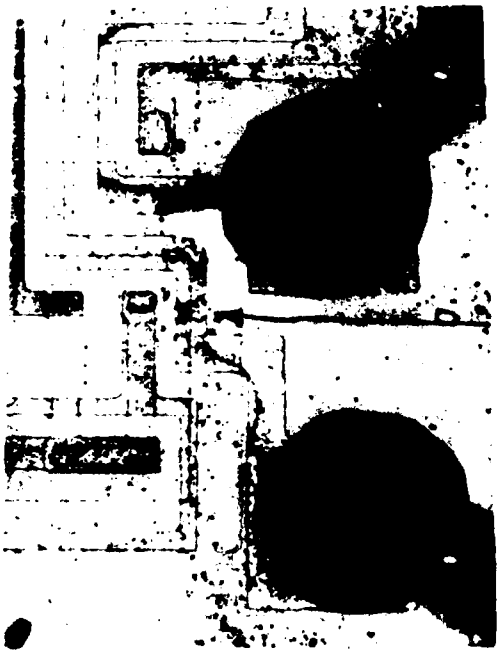
Figure 98

Device 5010

11

A-130X

Pad 11
Anodic
Corrosion



4

5

B-225X

MTC Indicated
Open Pin 5

Open Aluminum Run

Figure 99 Device 5023

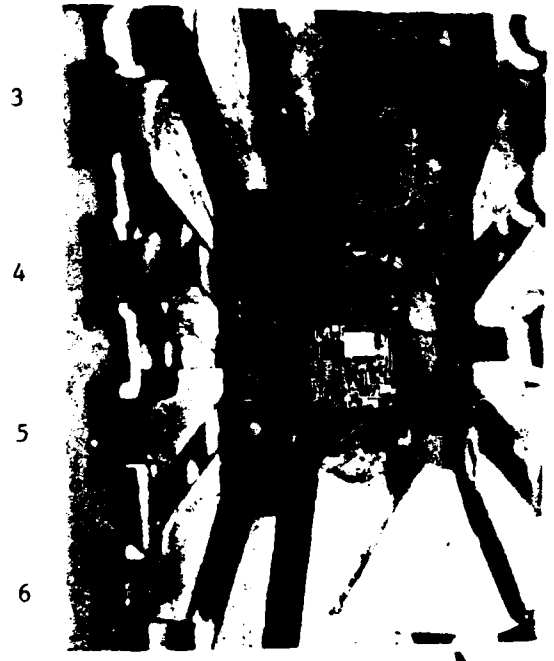
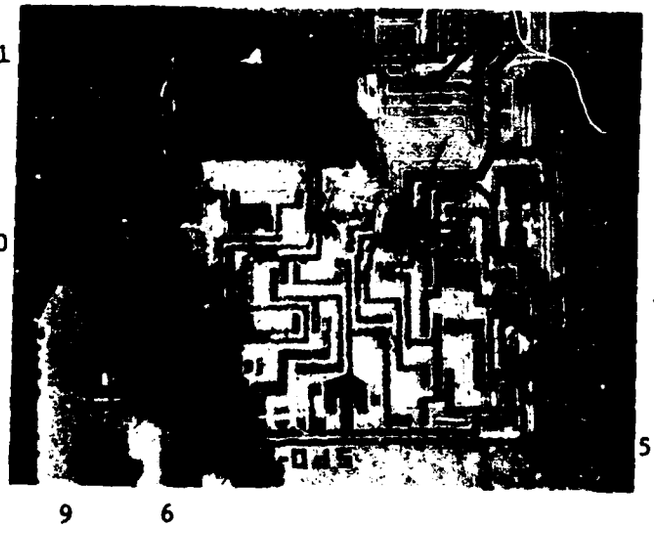


Figure 100 Device 5016 8X

A-50X

Device 5087

Zap from 11 to 6



B-50X

Device 5097

Zap from 11 to 6

Figure 101 Devices 5087, 5097

6. Test Cell 6 - Temperature Cycling Followed by Thermal Shock

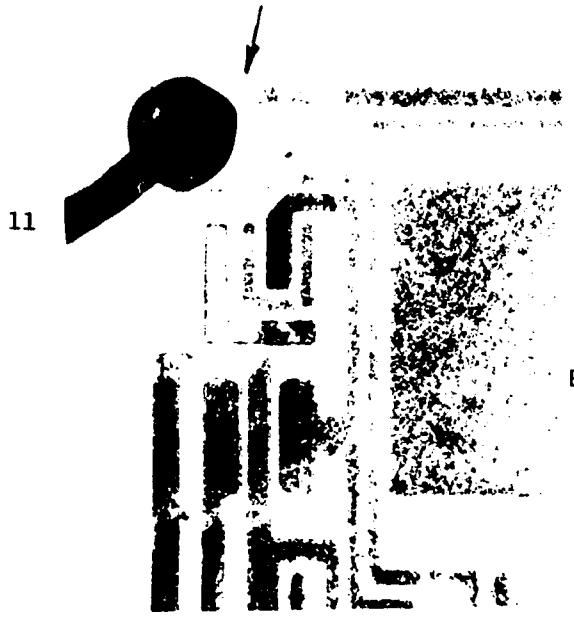
The primary failure mode for C Type devices subjected to the thermal shock sequence of stress was aluminum corrosion and loss of bond adhesion at the gold-aluminum interface. A summary of results of analyzing the failures from this stress is shown below. The devices had been inserted into liquid baths for temperature extremes, namely, ethylene glycol and dry ice and acetone. In spite of the relatively short periods of immersion, the liquid penetrated to the die in the failures.

Two devices with aluminum darkened slightly by surface corrosion or oxidation are shown in Figure 102. The aluminum metalization associated with Pin 11 in both devices was attacked severely and isolated completely from the circuits. Since this test was not run under electrical bias conditions, this preferential galvanic corrosion could only have taken place in the short intervals when Pin 11 was anodically biased for measurements with liquid in contact with internal metal structures.

The failed bonds at other pin sites were probably torn loose more by differential expansion stresses than by corrosion.

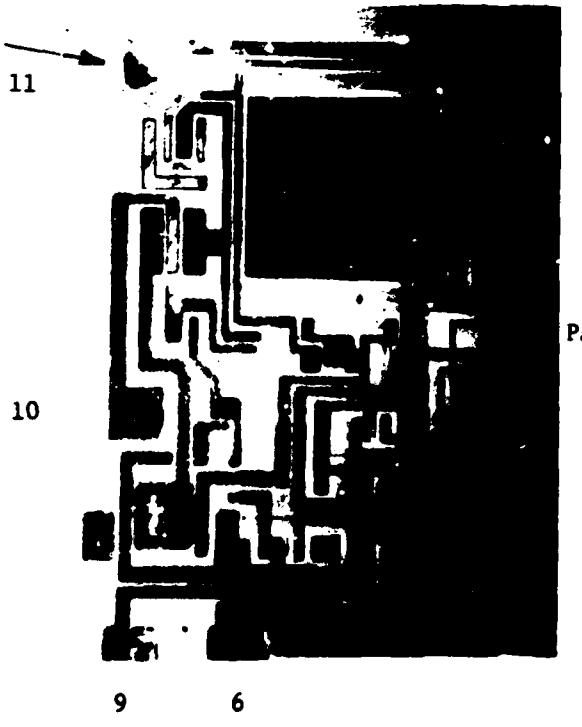
The E Type device failure 6066 was probably caused by Pad 5 to substrate leakage from silicon fracturing of the type seen in other stresses.

	Device Type	Electrical Defect
6007	C	Pin 11 - Open
6020	C	All parameters OK
6025	C	All pins intermittently open
6033	C	All pins intermittently open
6066	E	Leakage from Pin 5 to 6
6068	E	All parameters OK



A-120X

Device 6007
Pad 11 Corrosion



B-70X

Device 6025
Pad 11 Corrosion

Figure 102 Devices 6007, 6025

SECTION VI

CONCLUSIONS AND RECOMMENDATIONS

A scientifically and statistically sound program was designed and successfully executed to investigate and determine the basic failure mechanisms associated with linear microcircuits fabricated in ceramic and plastic packages. Devices from this accelerated stress program, which exceeded normal maximum device ratings, were evaluated and the failures were subjected to detailed failure analysis. Information from these evaluations provides critical information concerning the capabilities of state-of-the-art linear integrated circuits in several package configurations. The increased usage of linear microcircuits in a wide variety of functions in both commercial and military equipments makes the results of this program relevant.

The results from this program have brought out the strengths and weaknesses of both ceramic and plastic encapsulated microcircuits. In addition, information was provided concerning the relative merits of using different stresses and measurements on linear microcircuits. Some of the highlights from the program include the following results:

- The devices in ceramic packages Types A and B were comparable to plastic encapsulated devices Types C and D and superior to Type E under temperature step stress and electrical bias up to 200°C.

- Epoxy encapsulated devices and ceramic packaged devices were comparable on the salt atmosphere test. There was a higher number of failures of silicone encapsulated devices under this test.

- The plastic encapsulated and ceramic packaged devices were comparable on 1000 hours of humidity and temperature cycling with bias life

testing.

- The devices in ceramic packages Types A and B were comparable to plastic encapsulated devices Type D and superior to Types C and E under steady state humidity life with bias at 85°C, 85% R.H.

- Plastic encapsulated devices were in general superior to the ceramic packaged devices under thermal shock testing.

- The TEG failure occurrence correlates with the corresponding microcircuit failures, and they proved to be a more sensitive indicator of response to stress than the corresponding circuits.

- Monitored temperature cycling can be effective in screening out intermittent failures that escape detection when measured at room temperature. Care must be taken, however, that the monitored temperature cycle failure indications are due to the device under test and not a failure in the test system such as test cards.

- The 85°C, 85% humidity life test with bias proved to be a more severe test than the humidity with temperature cycling (25 to 65°C) with bias test.

A summary of the results from failure analysis includes:

- The predominant failure mechanism of the plastic encapsulated Type C devices was corrosion of the aluminum metalization under accelerated humidity and bias testing. However, the epoxy coated glassivated chips used in the gang bonded plastic encapsulated devices had almost no metal corrosion.

Type E failures from humidity and bias testing were primarily found to have latched-up or to have been subjected to overloads which destroyed circuit junctions and even inner lead frame structures in some cases. Initiation of the latch-up by moisture penetration is not a complete explanation since Type C units, with no latch-up failures reported, were penetrated by moisture to a greater extent than Type E devices. A complete explanation of this phenomena would require further investigations.

- Also failures of the plastic encapsulated Type E, ET devices under humidity life and temperature step stress with bias tests were due to mechanical or process induced fractures in the silicon under or near the pads. This reflects the results from state-of-the-art samples from early production in which the processes had not been completely optimized. These failures in general did not go into a runaway mode even though shorts had developed from bond pads to the substrate.

A diffusion technique could be used to minimize the electrical degradation caused by bond pad fractures such as described in Figure 86 for Type E devices and TRGs. An N type isolation window could be diffused in the silicon under all bond pads normally biased positively with respect to the substrate. A short from pad metalization to substrate due to fracturing or due to passivation pinholes would still be isolated from the circuit by a reverse biased diffused diode structure. Use of this technique would have reduced the Type E failures considerably.

The results from thermal shock testing indicated that there were no bond lift failures on the Type E devices as compared to some on the Type C devices, showing the greater bond strength for the gangbond method.

The majority of the ceramic packaged devices Type B failed under thermal

shock testing. The ethylene glycol used during thermal shock testing attacked the glass seal and caused failures. Most of the Type B devices that failed under the humidity and bias testing were related to cracking of the glassivation on the chip.

The information generated on this program can be utilized in the generation of test methods in MIL-STD-883, Test Methods and Procedures for Microelectronics. The following general conclusions can be made:

- The parameters, input offset voltage and power supply drain current, are sensitive indicators of linear microcircuit capabilities after accelerated stress testing,

- The salt atmosphere test requires about 48 hours of exposure to produce response,

- The test conditions of MIL-STD-883, Method 1004 are not as severe as 85°C, 85% RH,

- Steam pressure testing did not give an indication of future failures on humidity life and bias testing,

- The monitored temperature cycling test detected more failures during the elevated temperature excursion than during the low temperature portion of the cycle,

- The thermal shock test, liquid to liquid, was more severe than the temperature cycling, air to air, test.

The basic objective of this program has been met and the results were

very informative in showing the strengths and weaknesses of both the plastic and ceramic packaged microcircuits under accelerated test conditions. It also highlights the advantages of detailed failure analysis, which includes the utilization of the Scanning Electron Microscope. An area of further work and study would be to expand this work and evaluate new accelerated testing techniques and new plastic encapsulated devices. This would include the determination of the relationship between the accelerated tests used and the normal use conditions in applications.

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13. ABSTRACT

This final report describes the results obtained from a contract on a study of the reliability of linear integrated circuits. The objective of the contract was to investigate and determine the basic failure mechanisms associated with linear microcircuits fabricated in ceramic and plastic packages.

The type of test vehicle chosen for this program was the 741 operational amplifier. Two of the five vehicles chosen for the program were manufactured by one supplier with half of the devices encapsulated in ceramic packages and the other half encapsulated in silicone plastic. The devices fabricated by the other supplier included three packaging variations: the first was a ceramic package with conventional metallization and wire bonding, the second was a plastic encapsulated package with conventional metallization and wire bonding, and the third was a plastic encapsulated package utilizing a gang bonding technique. In addition, Test Element Groups (TEGs) were fabricated using the last three packaging techniques.

The test plan for these devices was designed to include both step-stress and long-term stress-in-time tests. The stresses were chosen to identify any failure mechanisms that could be activated by high temperatures, temperature cycling, salt atmosphere, steam pressure and high humidity environments. Over 1000 microcircuits and about 285 TEGs were measured for electrical parameters and then were stressed on this program. The device responses were analyzed during and after the stress program and representative candidates were then chosen for detailed failure analyses.

(more)

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13. Abstract (continued)

Summaries of the results of the stress tests and failure analyses along with the conclusions from these results are included in this report.